Regular Analog/RF Integrated Circuits Design Using Optimization With Recourse Including Ellipsoidal Uncertainty

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***Abstract*—Long design cycles due to the inability to predict silicon realities are a well-known problem that plagues analog/RF integrated circuit product development. As this problem worsens for nanoscale IC technologies, the high cost of design and multiple manufacturing spins causes fewer products to have the volume required to support full-custom implementation. Design reuse and analog synthesis make analog/RF design more affordable; however, the increasing process variability and lack of modeling accuracy remain extremely challenging for nanoscale analog/RF design. We propose a regular analog/RF IC using metal-mask configurability design methodology Optimization with Recourse of Analog Circuits including Layout Extraction (ORACLE), which is a combination of reuse and *shared-use* by formulating the synthesis problem as an *optimization with recourse* problem. Using a two-stage geometric programming with recourse approach, ORACLE solves for both the globally optimal shared and application-specific variables. Furthermore, *robust optimization* is proposed to treat the design with variability problem, further enhancing the ORACLE methodology by providing yield bound for each configuration of regular designs. The statistical variations of the process parameters are captured by a confidence ellipsoid. We demonstrate ORACLE for regular Low Noise Amplifier designs using metal-mask configurability, where a range of applications share common underlying structure and application-specific customization is performed using the metal-mask layers. Two RF oscillator design examples are shown to achieve robust designs with guaranteed yield bound.**

***Index Terms*—Configurable design, optimization with recourse, robustness, statistical optimization.**

I. Introduction

THE IC DESIGN and manufacturing costs are increasing to the point that fewer products have the volume required to amortize the large upfront nonrecurring engineering costs [1]. This is particularly the case for mixed-signal ICs that are designed in sub-100-nm technologies, where the technology advances are making application-specific system-on-chip designs technically feasible, but the economic realities require even higher product volumes. Design reuse and analog synthesis methodologies [2]–[7] have substantially addressed the design cost and risk challenges. For a given circuit topology and specifications, *simulation-based* optimization [2]–[4] and *equation-based* optimization [6], [7] have been effective for automating the design process. However, the large process parameter variability that is evident for nanoscale technologies along with the complex nature of parasitic coupling can cause the design risk, hence cost, to remain quite high, even for the best synthesis approaches.

For this reason, it is advantageous to design configurable analog/RF circuits [8], [9] that exploit circuit regularity. Importantly, such circuits can be precharacterized for the subtle device properties and coupling parasitics that are difficult to predict prior to layout and manufacturing. These regular analog/RF circuits reduce the design risk and accommodate the tight time-to-market windows. While the design cost of configurable circuits exploiting regularity can be high, the cost is shared over multiple applications.

We propose an *Optimization with Recourse of Analog Circuits including Layout Extraction* (ORACLE) methodology, which incorporates the shared-use and reuse benefits of configurable circuits, while offering performance that is comparable to a fully customized design. Instead of a flow to optimize a circuit for a single application, we propose an optimization framework that supports a methodology for configurable designs that "share" common structures. These common structures can then be precharacterized for subsequent application-specific customization, thereby allowing the second stage of optimization to accommodate extracted layout realities. We formulate our configurable design problem as an *optimization with recourse* problem. If we can formulate each of the sample problems (scenarios) as geometric programming (GP) problem [6], [7], the optimization with recourse problem can be then reduced to a two-stage GP with recourse (GPR) problem and solved efficiently.

Furthermore, to consider variability in the early stages of design exploration, we propose to formulate the design with variability problem as robust optimization, specifically robust

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GP, and capture the process variations using ellipsoidal uncertainty expression. The process variation issue has been treated by many statistical methods as classified in [10] into four broad categories: *direct yield optimization*, *design centering*, *worst-case optimization*, and *infinite programming*. The direct yield optimization [11], [12] aims at direct yield formulation or estimation through numerical integration or Monte Carlo analysis, often resulting prohibitive computational cost. The design centering approaches [13]–[15] try to find the design point furthest away from all constraint boundaries to be insensitive to process variations. Either lower bound (for maximal inscribed ellipsoid) or upper bound (for minimal circumscribed ellipsoid) of the actual parametric yield is estimated using this approach. The worst-case optimization techniques optimize worst-case circuit performances over all process and environmental variations (see, e.g., [16], [18]). Traditional worst-case optimization uses the process parameters taking values within a certain range which forms a tolerance "box," and the circuit performance is optimized for all of the "corners," or the vertices of the formed polyhedron. The state-of-the-art worst-case methods take the statistical distribution of the process parameters into consideration and evaluate the worst-case performance based on the probability density function (pdf) [10], [14], [16]. The robust GP proposed in this paper is one type of infinite programming, which attempts to minimize one cost function while satisfying all design constraints over the infinite set [19]. By formulation of optimization with ellipsoidal uncertainty, the statistical distribution information of both the process parameters and design variables can be included. More importantly, the problem size grows *linearly* with number of uncertain parameters in robust GP. Recent advances in robust optimization show that the robust GP with ellipsoidal uncertainty can be solved efficiently and accurately [20].

We demonstrate the ORACLE methodology by showing the numerical examples for the regular Low Noise Amplifier (LNA) designs using metal-mask configurability in SiGe and CMOS process. We further demonstrate the applications of the robust optimization formulation using two examples: a ring oscillator (RO) and an LC oscillator. The numerical results reveal that designs can be achieved with guaranteed yield bound, and the tradeoff curve of design cost and yield bound can be analyzed. It is shown that much less overdesign is achieved compared with the traditional corner-based optimization. We also include an example of silicon implementation of a back-end-of-line (BEOL) metal-mask configurable RF front end to validate this methodology [9].

The remainder of this paper is organized as follows. A brief overview of the regular analog/RF circuit design using metal-mask configurability is given in Section II. GP and Robust Optimization are introduced in Section III. Optimization with recourse and the ORACLE approach are introduced in Section IV. In Section V, we propose to formulate the design with variability problem as robust GP with ellipsoidal uncertainty, and the normal process variations are captured by the confidence ellipsoid. The numerical examples of regular LNA designs and robust optimization of RF oscillators are explained in Section VI, followed by conclusions in Section VII.

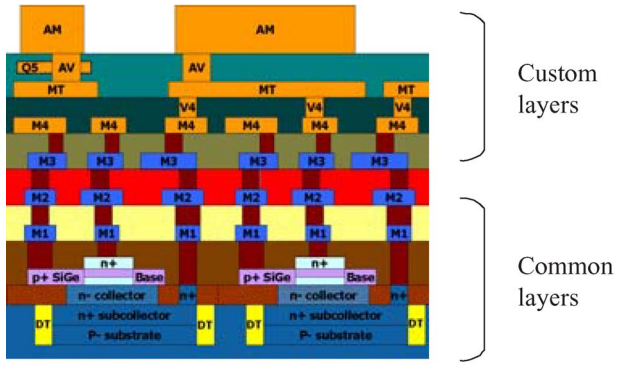

Fig. 1. Regular IC design via metal-mask configurability cross section.

II. Regular Analog/RF ICs Overview

Analog/RF IC designs are famous for the long design cycle and unpredictable parasitics. The analog/RF IC design iterations become more costly in nanoscale technology due to the mask set cost. Design reuse of regular structure such as BEOL metal-mask configurable circuit design can substantially address the design cost and risk challenges. It is suggested to divide the fabrication process into the device process and the metal patterning process. A common underlying base circuit, or *implementation fabric*, is designed to be shared across an entire spectrum of potential applications. The implementation fabric is optimized for manufacturability and accurately precharacterized in terms of devices and parasitics. A limited set of BEOL metal-masks are then used for application-specific customization, as depicted in the cross-sectional diagram of SiGe process in Fig. 1.

Our example implementation fabric described here includes RF components such as bipolar junction transistors (BJTs), MOSFETs, resistors, capacitors, and inductors. The customization of transistors (BJT or MOSFET) and resistors are realized by using a different number of multipliers. The spiral inductor and metal–insulator–metal capacitor are designed using top metal layers and hence fully customized for each application to minimize performance penalty. We chose to reserve a polysilicon patterned ground shield for inductor implementation which provides the lowest risk solution but incurs an area penalty. The metal-mask configuration for the various RF components is summarized in [9].

Traditional analog/RF IC design exploiting regularity is usually applied in an improvised way. In this paper, a systematic two-stage design methodology has been developed for determining both the optimal sizing of the implementation fabric for all possible applications and the optimal configuration for each individual application. This design methodology enables excellent control and characterization of devices and parasitics prior to final BEOL metal customization, thereby substantially lowering the design risk.

III. Mathematical Background

A. GP

Let $x_1, \ldots, x_n$ be n real, positive variables. We will denote the vector $(x_1, \ldots, x_n)$ of these variables as x. A function f is

called a *posynomial* function of x if it has the form

$$f(x_1,\ldots,x_n)=\sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}},\ldots,x_n^{\alpha_{nk}}$$

where $c_j \geq 0$ and $\alpha_{ij} \in \mathbf{R}$. Note that the coefficients c_j must be nonnegative, but the exponents α_{ij} can be any real numbers, including negative or fractional. When there is exactly one nonzero term in the sum, i.e., $t=1$ and $c_1>0$, we call f a *monomial* function.

A *geometric program* is an optimization problem of the form

$$\begin{array}{lll}\text{minimize} & f_0(x) & \\ \text{subject to} & f_i(x)\leq 1, & i=1,\ldots,m \\ & g_i(x)=1, & i=1,\ldots,p \\ & x_i>0, & i=1,\ldots, \end{array} \quad (1)$$

where $f_0,\ldots,f_{\mathrm{m}}$ are posynomial functions and $g_1,\ldots,g_p$ are monomial functions.

Note that the geometric program in (1) can be formulated as

$$\begin{array}{ll}\text{minimize} & c^{\mathrm{T}}y \\ \text{subject to} & \mathbf{lse}(A_{\mathrm{s}}y+b_{\mathrm{s}})\leq 0, \quad s=1,\ldots,m \end{array} \quad (2)$$

where the optimization variable is $y=\log x$ and $y\in\mathbf{R}^n$, the logarithm of coefficients in (1) become $c\in\mathbf{R}^n$, $A_{\mathrm{s}}\in\mathbf{R}^{K_{\mathrm{s}}\times n}$, $b_{\mathrm{s}}\in\mathbf{R}^{K_{\mathrm{s}}}$, and

$$\mathbf{lse}(y)=\log(e^{y_1}+\cdots+e^{y_k})$$

is called the *log-sum-exp* function. The geometric program is a convex optimization problem, i.e., the problem of minimizing a convex function subject to convex inequality constraints and linear equality constraints. This special type of convex optimization can be *globally* solved with *great* efficiency. We can use efficient interior-point methods to solve the problem, and there is a complete and useful duality, or sensitivity theory for it.

Recently, GP [35], [36] has found successful applications in the field of circuit design, e.g., [6], [33], [41], [43]. Many analog/RF circuit design problems have been successfully formulated as GP [6], [7] and solved with great efficiency. (See [36] and [42] for more complete lists of references.) Unlike simulation-based methods such as Simulated Annealing and Genetic Programming [3], [4], [17] which are often used in local optimization and stochastic optimization, GP-based convex optimization offers high speed and global optimality, while usually suffers the problem of long setup time and limited accuracy. Table I summarizes the performance comparison among the local optimization, the stochastic optimization, and the convex optimization used in analog synthesis methods.

TABLE I
COMPARISON OF ANALOG SYNTHESIS METHODS

Methods	Setup Time	Model Accuracy	Optimization Speed	Optimization Converge
Local Optimization	Small	High	Medium	Local Optimum
Stochastic Optimization	Small	High	Slow	Global Optimum
Convex Optimization	Large	Low	Fast	Global Optimum

B. Robust Optimization

The idea of robust optimization is to explicitly incorporate a model of data uncertainty in the formulation of an optimization problem. Various types of robust convex optimization problems, e.g., robust linear programs, robust quadratic programs, and robust semidefinite programs, have been proposed (see, e.g., [35], [37], [38], [39], and [40] for details).

A large class of robust optimization problems can be formulated as

$$\begin{array}{ll}\text{minimize} & \sup_{u\in\mathcal{U}} f_0(y,u) \\ \text{subject to} & \sup_{u\in\mathcal{U}} f_i(y,u)\leq 0, \quad i=1,\ldots,m \end{array} \quad (3)$$

where y is the optimization variable the same as in (2), u represents the uncertain problem data, the set $\mathcal{U}$ describes the uncertainty in u.

Note that the robust optimization problem (3) is a convex problem if f_i, $i=0,\ldots,m$ are convex in y for each $u\in\mathcal{U}$. Even so, its computational tractability depends on the particular functions f_i and the description of the uncertainty set $\mathcal{U}$. Therefore, choosing a good model for the uncertainty often involves a tradeoff between conservativeness and tractability. Most of the research in the area has therefore focused on formulating robust optimization problems that can be solved via convex optimization.

IV. ORACLE METHODOLOGY

A. Methodology Overview

In regular analog/RF designs, a common implementation fabric is shared by multiple applications through different configurations of metal-mask layers. Unlike optimization for a single application, the shared common structure can be well characterized via simulation or measurement before it is configured for multiple applications, thereby providing the predictability that is needed for a risk-free robust design. The proposed optimization infrastructure is applicable to configurable designs in general, but here is applied in regular analog/RF IC designs using metal-mask configurability, as shown in Fig. 2, to produce performance comparable to a fully customized application-specific design.

We select device design variables and metal-mask design variables as first stage design variables x and second stage design variables z, and the *scenario* is an application corresponding to a set of specifications. The design is accomplished in two stages: 1) optimal implementation fabric design and 2) optimal individual metal-mask design. In the first stage, we optimize the structure of the implementation fabric over a domain of multiple applications. Then, device and component properties are characterized via postsimulation or potentially on-wafer measurement. By doing this, we can use the extracted information to center the final design. In the second stage, accurate device and component models are plugged into the

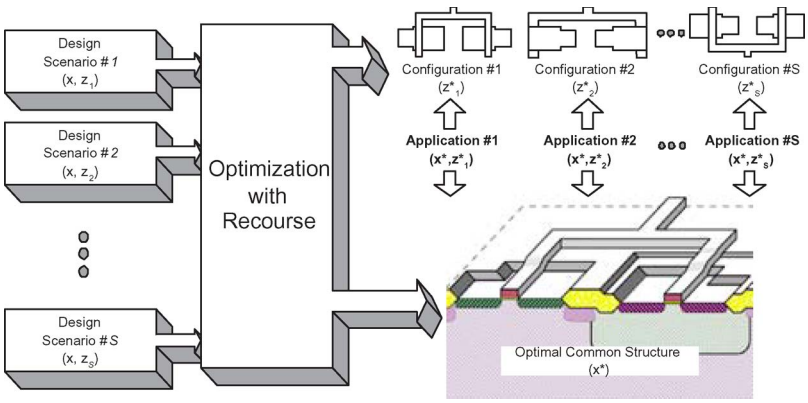

Fig. 2. ORACLE design methodology for regular analog/RF ICs.

original problem and resolved to achieve the individual metal-mask designs.

B. Problem Formulation

We formulate the regular analog/RF circuit design using metal-mask configurability as an optimization problem with recourse, also called *two-stage optimization* [22], [35], as shown in Fig. 2. In the two-stage optimization, we are to choose the values of two variables: $x \in \mathbf{R}^n$ and $z \in \mathbf{R}^q$, which in conjunction are the design variables for each of S applications, or *scenarios*. The variable x must be chosen *before* the particular scenario s is known; the variable z, however, is chosen *after* the value of the scenario random variable is known. In other words, z is a function of the scenario random variable s. To describe our choice z, we list the values we would choose under the different scenarios, i.e., we list the vectors

$$z_1, \ldots, z_{\mathrm{S}} \in \mathbf{R}^q.$$

Here, z_3 is our choice of z when $s = 3$ occurs, and so on. The set of values

$$x \in \mathbf{R}^n, \quad z_1, \ldots, z_{\mathrm{S}} \in \mathbf{R}^q$$

is called the *policy*, since it tells us what choice to make for x (independent of which scenario occurs), and also, what choice to make for z in each possible scenario. The variable z is called the *recourse variable* (or *second-stage variable*), since it allows us to take some action or make a choice after we know which scenario occurred. In contrast, our choice of x (which is called the *first-stage variable*) must be made without any knowledge of the scenario.

The cost function and constraints depend not only on our choice of variables, but also on a discrete variable $s \in \{1, \ldots, S\}$, which is interpreted as specifying which of S scenarios occurred. The cost function of each scenario is given by

$$f : \mathbf{R}^n \times \mathbf{R}^q \times \{1, \ldots, S\} \to \mathbf{R}$$

where $f(x, z_i, i)$ gives the cost when the first-stage choice x is made, second-stage choice z_i is made, and scenario i occurs. We will take the overall objective, to be minimized the average total cost over all policies, or to be minimized the maximum cost of all policies.

C. GPR

If each individual optimization problem can be formulated as a special type of convex optimization, namely, a GP, the optimization with recourse problem can be solved using a two-stage GPR approach.

Once individual optimization problems are formulated as GP, *Optimization with Recourse* can be solved by a two-stage GPR approach.

Suppose that the objective and constraint functions f are posynomial functions of (x, z), for each scenario $i = 1, \ldots, S$. In order to find an optimal policy, we must solve a GPR of the form

$$\begin{array}{lll} \text{minimize} & F_0(x, z_1, \ldots, z_{\mathrm{S}}) & \\ \text{subject to} & F_j(x, z_i) \le 1, \quad i = 1, \ldots, S, & j = 1, \ldots, m \\ & G_j(x, z_i) = 1, \quad i = 1, \ldots, S, & j = 1, \ldots, p \\ & x_i > 0, \quad i = 1, \ldots, n & \\ & z_i > 0, \quad i = 1, \ldots, q & \end{array} \tag{4}$$

where $F_j = \cup_{i=1}^{S} f(x, 0, \ldots, z_i, 0, \ldots)$ are posynomial functions for $j = 1, \ldots, m$, and $G_j = \cup_{i=1}^{S} f(x, 0, \ldots, z_i, 0, \ldots)$ are monomial functions for $j = 1, \ldots, p$. The new objective F_0 is the expected value of the total cost (or other cost functions which will be discussed later), and the new constraints are the union of all individual design constraints. The two-stage GPR problem can be treated as a much larger GP problem, since for each i, $f(x, z, i)$ can be transformed to be convex in (x, z_i), therefore linear-fractional functions preserve convexity.

The variables in the problem are $x, z_1, \ldots, z_{\mathrm{S}}$, i.e., the policy. The total dimension of the variables is $n + Sq$, compared with $n + q$ as in a single scenario case. The computational burden of solving the large geometric program equivalent for the original problem can be quite prohibitive. This is because we need to solve the set of $n + Sq$ (symmetric, positive definite) linear equations $\nabla^2 F \Delta_{nt} = -\nabla F$, where $F(x, z, i) = (F_0 \quad F_1 \quad \cdots \quad F_{\mathrm{m}})^{\mathrm{T}}$, which incurs a cost of approximately $(1/3)(n + Sq)^3$ flops. As a function of the number of scenarios, this grows like S^3.

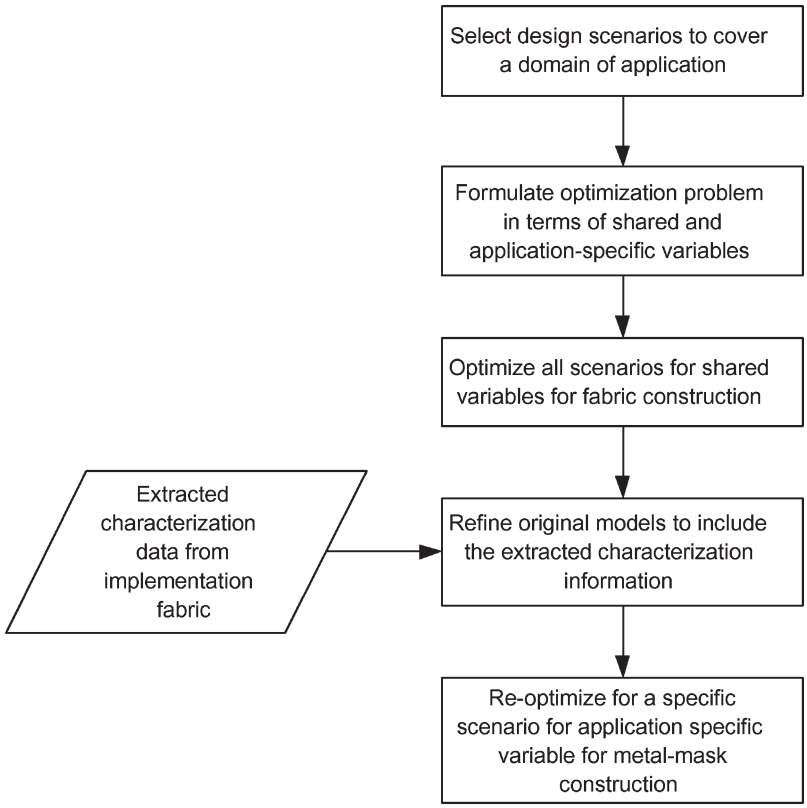

Fig. 3. ORACLE for metal mask configurable circuit flow chart.

Since a posynomial function f is a twice differentiable function of (x, z) for each scenario $i = 1, \ldots, S$, we can exploit the structure of the Hessian of $F(x)$ to compute the Newton step efficiently. Therefore, the overall complexity grows *linearly* [35] in S, and this scalability is an important feature of GPR.

Furthermore, since the GPR problem can be viewed as a much larger size GP problem, if it contains integer variables, we can use the same methods as discussed in solving MIGP problems to find the optimal solution of mixed integer GPR problems.

In the formulated optimization problem, the new constraints include all individual design constraints. While selecting the new objectives, we have several choices depending on the design goal. We can minimize the expected objective (average or weighted average), or the maximum objective among all scenarios, which would result in large margins for most scenarios. Another choice is to minimize the maximum *design surcharges*, which is defined as the performance difference between mask configurable design and the corresponding independent design. The independent design represents the full-custom design for each design scenario, and is therefore, the best we can achieve for each scenario under our optimization formulation. In this way, we can assess and minimize the cost to achieve mask configurability.

Since the GP formulation of each individual design is the basis for the GPR formulation of mask configurable design, in Section VI-A, we will describe the separation of design variables and list design constraints used in a single design GP formulation. Once the GP formulation of each design is obtained, the GPR formulation of the entire metal-mask configurable design can be readily obtained as previously discussed.

D. Practical Design Flow

In summary, regular analog/RF circuits can be used to reduce design risk and manufacturing cost. We proposed a novel design methodology and supporting optimization infrastructure for such configurable circuits. Fig. 3 shows the practical flow of applying ORACLE in the regular analog/RF IC design using metal-mask configurability.

A relatively coarse posynomial model is used in the fabric (first stage) design because we need to quickly explore large design spaces. The initial modeling inaccuracy can be corrected during the metal-mask (second stage) design through local design space fitting. Moreover, the extracted characterization information helps refining the devices and components model with parasitics included. The posynomial modeling accuracy in the second stage can be very high and the silicon reality can be much better predicted. By doing analog circuit design with recourse, we make analog computer-aided design no longer an open loop process and therefore a very practical design aid.

Unlike optimization for a single application, the shared common structure is well characterized via simulation or measurement before it is configured for multiple applications, thereby providing the predictability that is required for a risk-free robust design. Simulation-based posynomial fitting techniques [29], [43], [44] are particularly effective in our design methodology because the silicon implementation fabrics can be accurately modeled and characterized. By characterization of silicon and

posynomial models obtained by simulation, the mask design variables (the second-stage design variables) can be computed precisely, therefore the chances of first-silicon pass are greatly enhanced.

V. Capture Variability by Ellipsoid Uncertainty

A. Process Variation Sources and Modeling

The IC performance variability is impacted by two distinct sets of factors: *environmental factors* and *physical factors*. The environmental factors usually include variations in power supply voltage and temperature. The physical factors include variations in the electrical and physical parameters that characterize the behavior of active and passive devices, such as $V_{\rm th}$, $T_{\rm ox}$, $L_{\rm eff}$, etc. The process parameter variability can be measured through the ratio of the standard deviation (σ) and the mean value (μ). The increasing parameter variability of five technologies in the 250- to 70-nm gate length range is summarized in [21].

To consider those variability, we model process parameters as random variables with certain statistical distributions. We may use a uniform distribution over the range of the specifications for environmental factors. For example, the temperature can be modeled as a uniform distribution random variable from -25 °C to 125 °C. The physical parameters are typically represented by some joint pdf $N(\mu, \Sigma)$, where μ is a vector of means and Σ is a variance/covariance matrix. The correlation of those parameters cannot be ignored because of the mechanism of those parameters and the increasing impact of intradie variations.

B. Robust Optimization With Ellipsoidal Uncertainty

The circuit design with process variability problem can be cast as an optimization problem with a specific model uncertainty as in the robust optimization formulation (3). Therefore, to include the process variability in the early stage of design, we propose to formulate the circuit design with variability problem as robust GP, which can systematically incorporate a model of data uncertainty in a GP and optimize for all the given scenarios under this model. In addition, the various sources of variations are modeled as the ellipsoidal uncertainty.

To take into consideration some uncertainty or possible variation in the problem data $(A_{\rm s}, b_{\rm s})$ in (2) in a tractable manner, we assume that $(A_{\rm s}, b_{\rm s})$, $s = 1, \ldots, m$ are uncertain, but known to belong to the image of a set $\mathcal{U} \subset \mathbf{R}^L$ under the affine mapping

$$\left(\tilde{A}_{\rm s}(u), \tilde{b}_{\rm s}(u)\right) = \left(A_{\rm s}^0 + \sum_{j=1}^{L} u_j A_{\rm s}^j, b_{\rm s}^0 + \sum_{j=1}^{L} u_j b_{\rm s}^j\right) \quad (5)$$

where $A_{\rm s}^j \in \mathbf{R}^{K_{\rm s} \times n}$, $b_{\rm s}^j \in \mathbf{R}^{K_{\rm s}}$, $j = 0, \ldots, L$. The corresponding *robust* geometric program in *convex* form can then be formulated as

$$\begin{array}{ll} \text{minimize} & c^{\rm T} y \\ \text{subject to} & \sup_{u \in \mathcal{U}} \mathbf{lse}\left(\tilde{A}_{\rm s}(u) y + \tilde{b}_{\rm s}(u)\right) \le 0 \\ & s = 1, \ldots, m. \end{array} \quad (6)$$

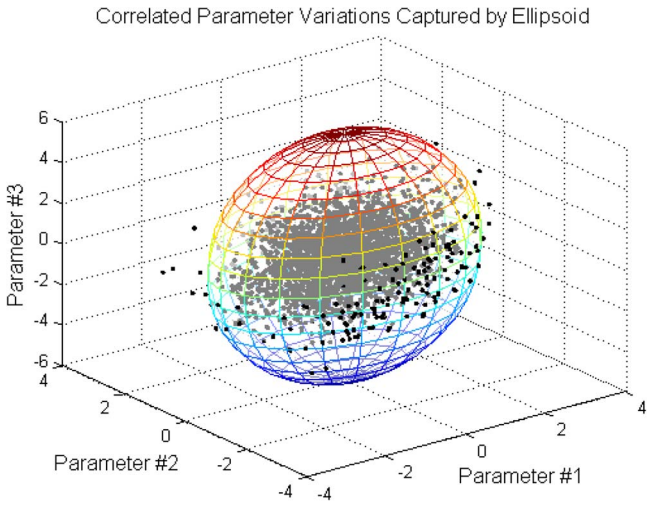

Fig. 4. Enclose correlated process variations by confidence ellipsoid.

In addition, in this paper, we assume that the robust GP (6) has *ellipsoidal uncertainty*, in which $\mathcal{U}$ is an ellipsoid

$$\mathcal{U} = \left\{\bar{u} + P\rho \,|\, \|\rho\|_2 \le 1, \rho \in \mathbf{R}^L\right\} \quad (7)$$

where $\bar{u} \in \mathbf{R}^L$ and $P \in \mathbf{R}^{L \times L}$.

It is not known whether the robust GP (6) with ellipsoidal uncertainty (7) can be reformulated as a tractable (convex) optimization problem. However, a tractable approximation method that yields a good compromise between solution accuracy and computational efficiency has been proposed. Refer to [20] for more details.

C. Confidence Ellipsoid

Recall that a normal random variable $u \in \mathbf{R}^n$ with mean $\bar{u}$ and positive definite covariance matrix $\Sigma = \Sigma^{\rm T} > 0$, i.e., $u \sim \mathcal{N}(\bar{u}, \Sigma)$, has the pdf

$$p_{\rm u}(\xi) = (2\pi)^{-n/2} (\det \Sigma)^{-1/2} e^{-1/2(\xi - \bar{u})^{\rm T} \Sigma^{-1} (\xi - \bar{u})}. \quad (8)$$

Obviously, $p_{\rm u}(\xi)$ is constant for $(\xi - \bar{u})^{\rm T} \Sigma^{-1} (\xi - \bar{u}) = \gamma$, i.e., on the surface of ellipsoid

$$\mathcal{E}_\gamma = \left\{\xi | (\xi - \bar{u})^{\rm T} \Sigma^{-1} (\xi - \bar{u}) \le \gamma\right\}. \quad (9)$$

Here, $\mathcal{E}_\gamma$ is called a *confidence ellipsoid* of u. It is well known that the nonnegative random variable $(u - \bar{u})^{\rm T} \Sigma^{-1} (u - \bar{u})$ has a chi-squared distribution with degree n, i.e.,

$$\mathbf{Prob}(u \in \mathcal{E}_\gamma) = F_{\chi_n^2}(\gamma) \quad (10)$$

where $F_{\chi_n^2}$ is the cumulative distribution function of χ_n^2.

If the process variations are normally distributed with the density function (8), a prespecified amount of mass of probability $0 < \alpha < 1$ can be captured by the confidence ellipsoid $\mathcal{E}_\gamma$ (9) with $\alpha = F_{\chi_n^2}(\gamma)$, as shown in Fig. 4.

D. Yield-Guaranteed Robust Design

Suppose the uncertainty parameter $u \in \mathbf{R}^L$ in the robust GP (6) is *random* and normally distributed with the density function

(8). Given $0 < \alpha < 1$, we say that $\hat{y} \in \mathbf{R}^n$ has *yield* no lower than α if

$$\mathbf{Prob}\left(\mathbf{lse}\left(\tilde{A}_i(u)\hat{y} + \tilde{b}_i(u)\right) \le 0, \qquad i = 1, \ldots, m\right) \ge \alpha.$$

The yield-guaranteed robust design can be obtained by letting the ellipsoidal uncertainty set $\mathcal{U}$ defined in (7) to be the confidence ellipsoid $\mathcal{E}_\gamma$ define in (9). Then, all the feasible solutions of the robust GP (6) have yield no lower than $F_{\chi_n^2}(\gamma)$. Therefore, in the robust GP framework, we can capture both the independent and the correlated normal randomness by the ellipsoidal uncertainty (9), and the resulting feasible solutions always have guaranteed yield bound $F_{\chi_n^2}(\gamma)$.

E. Implementation Issues

In this section, we first show that narrow normal distributions can be approximated by lognormal approximations. Then, we give the generic formulation of GP in posynomial form with incorporated process variations. Based on the lognormal approximation of narrow normal distribution, the robust design with guaranteed yield bound can be achieved by reformulating the GP in posynomial form with normal variations as the robust GP (6) with the ellipsoidal uncertainty (9).

1) Approximate Narrow Normal Distributions by Lognormal Distributions: Let u be normally distributed with mean μ and variance σ^2. Assume that u is *narrow*, i.e., $\sigma \ll \mu$; therefore, the mass of probability of u is mostly concentrated in the small interval $[\mu - 3\sigma, \mu + 3\sigma]$. To approximate the narrow normal random variable u by a lognormal random variable, of which pdf is defined on *positive* real numbers, here, we assume $\mu - 3\sigma > 0$ such that most of u (with high probability) is distributed within a positive interval. Therefore, for all $\xi \in [\mu - 3\sigma, \mu + 3\sigma]$, we have $\log(\xi/\mu) \simeq \xi/\mu - 1$, since $\xi/\mu \simeq 1$. Furthermore, for all $\xi \in [\mu - 3\sigma, \mu + 3\sigma]$

$$\begin{aligned} p_{\mathrm{u}}(\xi) &= (2\pi)^{-1/2}\sigma^{-1}e^{-(\xi-\mu)^2/(2\sigma^2)} \\ &\simeq (2\pi)^{-1/2}\left((\sigma/\mu)\xi\right)^{-1} e^{-(\log\xi - \log\mu)^2/(2(\sigma/\mu)^2)}. \end{aligned}$$

Therefore, *narrow* normal distributions can be approximated by lognormal distributions

$$\sigma \ll \mu: \quad \mathcal{N}(\mu, \sigma^2) \simeq \mathcal{LN}\left(\log\mu, (\sigma/\mu)^2\right). \tag{11}$$

(Recall that a random variable v has the lognormal distribution $v \sim \mathcal{LN}(\mu_v, \sigma_v^2)$ if its pdf has the form

$$p_v(\xi) = \frac{1}{\sqrt{2\pi}\sigma_v}\frac{1}{\xi}e^{-(\log\xi - \mu_v)^2/\left(2\sigma_v^2\right)} \tag{12}$$

where $0 < \xi < \infty$, $-\infty < \mu_v < \infty$, and $\sigma_v > 0$.) For example, the normal distribution $\mathcal{N}(4.5\text{ nm}, (0.1\text{ nm})^2)$ of T_{ox} can be approximated as a lognormal distribution with less than 1.3% error. (The proof of generic lognormal approximations of normal distributions can be found in [34].)

2) Incorporate Process Variations in GP of Posynomial Form: Many optimization-based circuit designs result in geometric programs of *posynomial* form. When process variations are incorporated, the robust design with guaranteed yield bound can be formulated as the following optimization problem:

$$\begin{aligned} &\text{minimize} \quad c^{\mathrm{T}}x \\ &\text{subject to} \quad \mathbf{Prob}\left(f_{\mathrm{s}}(x,p) \le 1, \qquad s = 1, \ldots, m\right) \ge \alpha \end{aligned} \tag{13}$$

where $0 < \alpha < 1$ is the required yield bound, $x \in \mathbf{R}^{n_x}$ are the design variables, $p \in \mathbf{R}^{n_p}$ represents the process parameters, and

$$f_{\mathrm{s}}(x,p) \triangleq \sum_{k=1}^{K_{\mathrm{s}}}\left(d_{ks}\prod_{i=1}^{n_p}(p_i + \delta p_i)^{b_{iks}}\prod_{j=1}^{n_x}(x_j + \delta x_j)^{a_{jks}}\right). \tag{14}$$

Here, the process variations in the process parameter p_i and design variable x_i are modeled by the random variables δp_i and δx_i, respectively. Another implicit assumption is that $f_{\mathrm{s}}(x,p)$ is posynomial in x and p when we let $\delta p_i = 0$, $i = 1, \ldots, n_p$ and $\delta x_j = 0$, $j = 1, \ldots, n_x$.

a) Variance-linked-to-mean variations in process parameters: Consider the robust design (13) with required yield bound α. Assume that $\delta x_j = 0$, $j = 1, \ldots, n_x$ in (14), i.e., no variation in the design variables. We model the variance-linked-to-mean normal variations in process parameters by

$$\delta p_i/p_i \sim \mathcal{N}\left(0, \sigma_{p_i}^2\right), \qquad i = 1, \ldots, n_p$$

where $\sigma_{p_i} \ll 1$, $i = 1, \ldots, n_p$ are given. Let $\Sigma_p = \Sigma_p^{\mathrm{T}} > 0$ be the covariance matrix of $\delta p_i/p_i$, $i = 1, \ldots, n_p$. For values of δp_i with high probability, $f_{\mathrm{s}}(x,p)$ can be inferred as follows:

$$\begin{aligned} f_{\mathrm{s}}(x,p) \simeq \sum_{k=1}^{K_{\mathrm{s}}}\exp\Bigg[&\left(c_{ks} + \sum_{i=1}^{n_p} b_{iks}q_i\right) \\ &+ \sum_{i=1}^{n_p} b_{iks}u_i + \sum_{j=1}^{n_x} a_{jks}y_j\Bigg] \end{aligned} \tag{15}$$

in which $c_{ks} = \log d_{ks}$, $q_i = \log p_i$, $u_i = \delta p_i/p_i$, and $y_j = \log x_j$. Therefore, $f_{\mathrm{s}}(x,p) \le 1$ can be easily reformulated as a log-sum-exp constraint

$$\mathbf{lse}\left(\left(A_{\mathrm{s}}^0 + \sum_{j=1}^{n_p} u_j A_{\mathrm{s}}^j\right)y, b_{\mathrm{s}}^0 + \sum_{j=1}^{n_p} u_j b_{\mathrm{s}}^j\right) \le 0 \tag{16}$$

with appropriate A_{s}^j and b_{s}^j, $j = 0, \ldots, n_p$. We can reformulate each constraint $f_{\mathrm{s}}(x,p) \le 1$ of (13) in form of the above

log-sum-exp constraint and then obtain a robust GP of the form (6) with the ellipsoidal uncertainty

$$\mathcal{U} = \left\{ u \in \mathbf{R}^{n_p} | u^{\mathrm{T}} \Sigma_p^{-1} u \leq \gamma \right\} \tag{17}$$

where γ satisfying $F_{\chi_n^2}(\gamma) = \alpha$. Assume that $\hat{y} \in \mathbf{R}^{n_x}$ is a feasible solution of the resulting robust GP. Then, $\hat{x}_j = e^{\hat{y}_j}$, $j = 1, \ldots, n_x$ satisfy (13), i.e., $\hat{x} \in \mathbf{R}^{n_x}$ has yield no lower than α.

b) Variance-not-linked-to-mean variations in design variables and process parameters: Consider the robust design (13) with required yield bound α. Assume that the upper and lower bounds for each design variable are given

$$0 < L_j \leq x_j \leq U_j, \qquad j = 1, \ldots, n_x. \tag{18}$$

We model the variance-not-linked-to-mean, normal variations in process parameters and design variables by

$$\begin{aligned} \delta p_i &\sim \mathcal{N}\left(0, \sigma_{p_i}^2\right), \qquad i = 1, \ldots, n_p \\ \delta x_j &\sim \mathcal{N}\left(0, \sigma_{x_j}^2\right), \qquad j = 1, \ldots, n_x. \end{aligned}$$

Here, we assume that $\sigma_{p_i} \ll p_i$, $i = 1, \ldots, n_p$. In addition, we assume that $\sigma_{x_j} \ll x_j$, $j = 1, \ldots, n_x$. (Note that, in general, we can verify if this assumption holds since in many circuit designs it is easy to determine reasonable range of values for each design variable, e.g., (18).) We also assume that $p_i - 3\sigma_{p_i} > 0$, $i = 1, \ldots, n_p$ and $x_j - 3\sigma_{x_j} > 0$, $j = 1, \ldots, n_x$. Therefore, by (11)

$$\begin{aligned} p_i + \delta p_i &\simeq \mathcal{LN}\left(\log p_i, (\sigma_{p_i}/p_i)^2\right), \qquad i = 1, \ldots, n_p \\ x_j + \delta x_j &\simeq \mathcal{LN}\left(\log x_j, (\sigma_{x_j}/x_j)^2\right), \qquad j = 1, \ldots, n_x. \end{aligned}$$

Recall that a lognormal random variable $v \sim \mathcal{LN}(\mu, \sigma^2)$ can be inferred from $v = e^{\mu + \sigma u}$ with $u \sim \mathcal{N}(0, 1)$. Then, $f_{\mathrm{s}}(x, p)$ can be inferred from

$$\begin{aligned} f_s(x,p) &\simeq \sum_{k=1}^{K_i} \exp\left[\left(c_{ks} + \sum_{i=1}^{n_p} b_{iks} q_i \right) \right. \\ &\quad + \left(\sum_{i=1}^{n_p} b_{iks} \frac{\sigma_{p_i}}{p_i} u_i + \sum_{j=1}^{n_x} a_{jks} \sigma_{x_j} \alpha_j \hat{u}_j \right) \\ &\quad \left. + \sum_{j=1}^{n_x} a_{jks} y_j + \sum_{j=1}^{n_x} a_{jks} \sigma_{x_j} \beta_j \hat{u}_j y_j \right] \end{aligned} \tag{19}$$

in which $c_{ks} = \log d_{ks}$, $q_i = \log p_i$, and $y_j = \log x_j$. Here, $u_i \sim \mathcal{N}(0, 1)$, $i = 1, \ldots, n_p$ and $\hat{u}_j \sim \mathcal{N}(0, 1)$, $j = 1, \ldots, n_x$; $\alpha_j + \beta_j y_j$, $j = 1, \ldots, n_x$ are linear approximations of e^{-y_j} subject to $y_j \in [\log L_j, \log U_j]$, $j = 1, \ldots, n_x$, respectively. (Many methods, e.g., least-square fitting, can be used to find good linear approximations for e^{-y_j} within the interval $[\log L_j, \log U_j]$.) Therefore, we can reformulate each constraint $f_{\mathrm{s}}(x, p) \leq 1$ in (13) as a log-sum-exp constraint [like (16)] to obtain a robust GP of the form (6) with the ellipsoidal uncertainty

$$\mathcal{U} = \left\{ \xi = (u, \hat{u}) | \xi^{\mathrm{T}} \Sigma_\xi^{-1} \xi \leq \gamma, \xi \in \mathbf{R}^{n_p + n_x} \right\} \tag{20}$$

where γ satisfying $F_{\chi_n^2}(\gamma) = \alpha$, and $\Sigma_\xi = \Sigma_\xi^{\mathrm{T}} > 0$ is the covariance matrix of u_i, $i = 1, \ldots, n_p$ and $\hat{u}_j$, $j = 1, \ldots, n_x$. Assuming $\hat{y} \in \mathbf{R}^{n_x}$ is a feasible solution of the resulting robust GP, then $\hat{x}_j = e^{\hat{y}_j}$, $j = 1, \ldots, n_x$ satisfy (13), i.e., $\hat{x} \in \mathbf{R}^{n_x}$ has yield no lower than α.

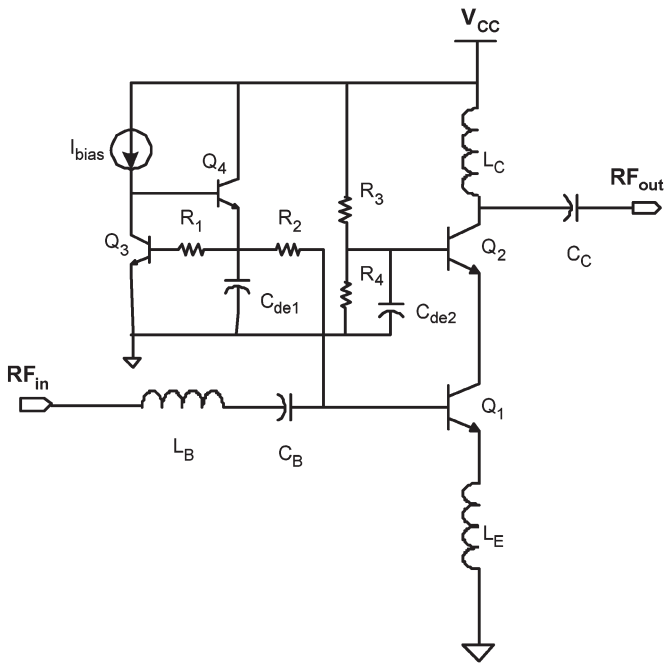

Fig. 5. Simplified SiGe LNA schematic.

VI. Regular RFIC Design Examples

A. Regular LNA Design Using Metal-Mask Configurability

An LNA is an important building block for any RF or wireless receiver. Depending on the system requirements, different technologies may be used for LNA designs. SiGe has been a promising process for future wireless communication systems due to the quality of having a higher performance compared to CMOS at lower price compared to GaAs, and is readily integrated with standard CMOS devices. Therefore, we will use a SiGe LNA example to illustrate the detailed optimization procedure of regular design using metal-mask configurability. Then, the numerical results of regular CMOS LNA will also been shown.

1) Design Problem: The specific SiGe LNA topology we consider in this paper is shown in Fig. 5. This topology has been widely used due to its lower noise performance compared with other topologies [24]. This circuit consists of an input tune loop followed by a cascode common-emitter transconductance stage with tuned output loop. Since the LNA is part of an RF front end, it is also required to match the impedance with input and output to maximize power transfer.

2) Design Variables: There are 12 independent physical variables in a single design that we would like to optimize for

the simplified SiGe LNA design. These design variables are related to the sizing and biasing of the input BJT and inductors. The cascode transistor Q_2, the dc biasing circuitry (R_1, R_2, R_3, R_4, Q_3, and Q_4), and decoupling capacitors ($C_{\rm d1}$ and $C_{\rm d2}$) are heuristically sized for best matching and power consumption performance.

The 12 independent design variables are divided into two categories: *device design variables* and *metal-mask design variables*, which correspond to the front end and the back-end of the SiGe fabrication processes.

1) Device design variables: the emitter length $l_{\rm E}$ and width $w_{\rm E}$ of input transistor Q_1, and the outer dimension D_1, D_2, D_3 of three inductors $L_{\rm E}$, $L_{\rm B}$, and $L_{\rm C}$. These variables are restricted to take values on a discrete grid. Since the layout grid in modern technology is very small, we ignore the grid constraints in this paper and consider these variables to be *positive real numbers*.
2) Metal-mask design variables: m_1 is the number of devices of the same geometry used in parallel for input BJT, which should be *integer number*; the number of turns n_1, n_2, n_3 of three inductors, which would be *integer multipliers* of 0.25 (quarter turns); the value of the input and output tune capacitors $C_{\rm B}$ and $C_{\rm C}$, and the collector current $I_{\rm C}$, which is considered as *positive real numbers*.

There are a number of parameters that we consider fixed, e.g., the supply voltages $V_{\rm cc}$ and gnd, and the various process and technology parameters associated with the SiGe models.

3) Design Specifications and Parameters: In order to cast the design of LNAs as GP, we need to show that the LNA design specifications can be posed as posynomial functions of the design variables. Being able to write circuit equations in posynomial form is the key to use GP to design analog circuits. To achieve equations in posynomial form, one needs to make reasonable approximations. Since our equations show excellent agreement with simulation results, we conclude that our approximations are valid.

The LNA was designed to achieve simultaneous noise and power match using the method reported in [24], [25], and [26]. Under the power consumption constraint, it is desirable to achieve gain with input and output impedance match, while maintaining the minimum noise and distortion level, also minimizing the silicon area. Therefore, when formulating the GP problem, we minimize area subject to the following constraints:

1) noise match;
2) input impedance match;
3) gain requirement;
4) output impedance match;
5) nonlinear distortion requirement;
6) power constraint.

We use the Gummel-Poon BJT model to derive the initial design equations, where electrical elements in this model are monomial expressions of physical design variables. A simple monomial fitting [35] technique can be employed to fit the VBIC95 [46] BJT model to achieve better accuracy. For on-chip inductors, all the elements in the lumped electrical model can be expressed as monomial or posynomial function of layout variables, as shown in [7] and [27].

The design parameters considered in the LNA design is the center frequency ω_0 and source impedance $R_{\rm s}$, which is usually 50 Ω in RF systems.

4) Design Equations:

a) Noise match: The authors of [26] showed that the minimum achievable NF for a bipolar device in a common-emitter configuration when matched to its optimum noise figure source impedance is given by

$$\mathrm{NF}_{\min}(J_{\rm C}) = 1 + \frac{n}{\beta_{\rm DC}} + \sqrt{aJ_{\rm C} + b + \frac{c}{J_{\rm C}}} \tag{21}$$

where

$$a = \frac{2}{V_{\rm T}}(r_{\rm b} + r_{\rm e})_{\rm u}\left(4\pi^2\tau_{\rm F}^2 f^2 + \frac{1}{\beta_{\rm DC}}\right) \tag{22}$$

$$b = 16\pi^2\tau_{\rm F}(r_{\rm b} + r_{\rm e})_{\rm u}(C_{\rm je} + C_{\rm jc})_{\rm u} f^2 + \frac{n^2}{\beta_{\rm DC}} \tag{23}$$

$$c = 8\pi^2 V_{\rm T}(r_{\rm b} + r_{\rm e})_{\rm u}(C_{\rm je} + C_{\rm jc})_{\rm u} f^2 \tag{24}$$

where $(r_{\rm b} + r_{\rm e})_{\rm u}$ are the base and emitter ohmic resistance of a unit device, $(C_{\rm je} + C_{\rm jc})_{\rm u}$ are the base-emitter and base-collector junction capacitance for a unit device, respectively. $J_{\rm C}$ is the dc collector current density, $V_{\rm T}$ is kT/q, $\beta_{\rm DC}$ is the collector-base dc current gain, f is the frequency of operation, and n is the junction grading factor ranging from 1 to 1.2. To simplify the analysis, $\beta_{\rm DC}$, $(r_{\rm b} + r_{\rm e})_{\rm u}$, $(C_{\rm je} + C_{\rm jc})_{\rm u}$, n are assumed to be constant as a function of collector current density. This is a valid assumption since the device is usually biased at current densities considerably below peak $f_{\rm T}$, and these parameters varies little with collector current.

For frequencies well below $f_{\rm T}$, the minimal collector current density can be approximated to be

$$J_{\rm C-opt} \approx 2\pi(C_{\rm je} + C_{\rm jc})_{\rm u} V_{\rm T}\sqrt{\beta_{\rm DC}} f \tag{25}$$

where $J_{\rm C-opt}$ scales linearly with the operating frequency. This is an important result to achieve scalable design for multiband systems.

b) Input impedance match: The input impedance is given by [24] and [25] as

$$Z_{\rm in} = j\omega(L_{\rm E} + L_{\rm B}) + R_{\rm b} + \frac{1}{j\omega C_{\rm in}} + 2\pi f_{\rm T} L_{\rm E} \tag{26}$$

where $L_{\rm E}$, $L_{\rm B}$ are the emitter and base inductances, respectively; $R_{\rm b}$ is the BJT external base resistance, $C_{\rm in}$ is the capacitance looking into the base of the amplifier; $g_{\rm m}$ is the BJT transconductance. The inductor parasitic resistance is ignored here. By observing the input impedance of the amplifier with the emitter degenerated inductor, we simply see a real and an imaginary part. The real part is a function of Q_1 sizing and biasing. The emitter inductor $L_{\rm E}$ is used to match the real part of the input impedance to $R_{\rm S}$ (typically 50 Ω). This is a monomial equality constraint

$$L_{\rm E} \cong \frac{R_{\rm S}}{2\pi f_{\rm T}} = R_{\rm S}\left(\tau_{\rm F} + V_{\rm T}\frac{(C_{\rm je} + C_{\rm jc})_{\rm u}}{J_{\rm C}}\right). \tag{27}$$

Simultaneous noise and input impedance match is finally obtained by the base inductor $L_{\rm B}$. It cancels out the reactance due to the input capacitance $C_{\rm in}$ of the device, and, at the same time, it transforms the optimum noise reactance of the amplifier to 0 Ω. The source reactance is

$$X_{\rm in} = 2\pi f(L_{\rm E} + L_{\rm B}) - \frac{1}{\omega_0 C_{\rm in}}. \tag{28}$$

Ideally, this part should be 0 Ω exactly. However, due to our model accuracy and implementation reality, we put a boundary to make it capacitive, and this is translated into a posynomial inequality constraint

$$\omega_0^2(L_{\rm E} + L_{\rm B})C_{\rm in} \leq 1. \tag{29}$$

c) Gain: The total voltage gain of the whole system is

$$A_{\rm v} = Q_{\rm in}\frac{g_{\rm m1}}{g_{\rm o}} \tag{30}$$

where $Q_{\rm in}$ is the quality factor of the input loop, $g_{\rm o}$ is the output conductance of the transistor

$$Q_{\rm in} = \frac{1}{2\pi f R_{\rm s} C_{\rm in}} \tag{31}$$

$$g_{\rm o} = \frac{g_{\rm o2}g_{\rm o1}}{g_{\rm m2}} + \frac{R_{\rm d}}{4\pi^2 f^2 L_{\rm d}^2} \tag{32}$$

where $R_{\rm d}$ is the transformed version of the parasitic resistor of the inductor.

It follows that the gain requirement will be represented as a posynomial inequality constraint:

$$\frac{2\pi f R_{\rm s} C_{\rm in}}{g_{\rm m1}}\left(\frac{g_{\rm o2}g_{\rm o1}}{g_{\rm m2}} + \frac{R_{\rm d}}{4\pi^2 f^2 L_{\rm d}^2}\right) \leq \frac{1}{G_{\min}}. \tag{33}$$

d) Output impedance match: To maximize output power transfer, we try to match the output impedance to the load. Normally we use an extra shunt capacitor $C_{\rm C}$ to form output match network.

The output impedance of the tune loop would be

$$Z_{\rm out} = j2\pi f L_{\rm C} + \frac{1}{j2\pi f C_{\rm C}} + R_{\rm C} \tag{34}$$

where $L_{\rm C}$ is the collector inductances; $R_{\rm C}$ is the equivalent parallel resistance of the collector inductor.

The real part of the output impedance would match the load impedance, therefore, $R_{\rm C} = R_{\rm S}$, which is a monomial equality constraint.

The imaginary part can be inductive or capacitive. We will also put a boundary for that to make sure that it never gets capacitive. The imaginary part at the operating frequency f is as follows:

$$X_{\rm out} = 2\pi f L_{\rm C} - \frac{1}{\omega_0 C_{\rm out}} \tag{35}$$

and the constraint to make it capacitive is a posynomial inequality constraint

$$\omega_0^2 L_{\rm C} C_{\rm out} \leq 1. \tag{36}$$

TABLE II
OPTIMAL TWO-STAGE VARIABLES FOR 2.1-GHz SiGe LNA

Variables	Value
w_E	0.32μm
l_E	2.5μm
D_1	200μm
D_2	250μm
D_3	300μm
m_1	48
I_{bias}	600μA
C_C	0.41pF
C_B	6.65pF
n_1	1.75
n_2	3.5
n_3	5.5

e) Nonlinear distortion: The LNA nonlinear distortion is measured in terms of input-referred third-order intercept point (IIP3). A close form of IIP3 is difficult to obtain since the nonlinearity of all components contributes to the total distortion. It is usually recommended to use a posynomial fitting method to get the IIP3 expression [29], [43]. However, the authors in [28] found the relation of IIP3 and the biasing current. The third-order intermodulation (IM3) can be approximated as

$$|IM_3| \propto \left|\frac{A_1(2\pi f)}{I_{\rm C}}\right|^3 \tag{37}$$

where $A_1(2\pi f)$ denotes the first Volterra series coefficient. We can see that the $|IM_3|$ is proportional to the cube of the inverse of the bias current $(I_{\rm C})$. By putting a lower bound of IM3 (or an upper bound of IIP3), we can find the minimum bias current needed, which is another monomial inequality constraint.

f) Power constraint: Power is critical in LNA design. We set the sizing ratio of input BJT and bias BJT to be N. The power consumption can be approximated by

$$P = V_{\rm cc}I_{\rm c}\left(1 + \frac{1}{N}\right).$$

If we put an upper bound on the power consumption, it would result in another monomial constraint.

5) Numerical Results of SiGe LNAs: We use a 47-GHz $f_{\rm T}$ NPN BJT SiGe BiCMOS process to demonstrate ORACLE on some LNA examples. The positive supply voltage was set at 2.5 V, and the negative supply voltage was set at 0 V.

a) Independent design and verification: We use the design variables described in Section VI-A2 and design constraints listed in Section VI-A3 for a SiGe LNA example with 2.1-GHz center frequency. The resulting geometric program has 12 variables, and 28 inequality constraints. The formulated GP problem was solved efficiently by the MOSEK toolbox [23] on the order of a millisecond. The optimal design obtained is shown in Table II.

The target specifications and the performance achieved by this design, as predicted by the program, are summarized in Table III. For a given circuit topology and a set of design specifications, this is the best we can get and used as the benchmark. Note that some constraints are tight (power consumption, center frequency and gain), while some constraints are not (Noise figure, S-parameters, and IIP3).

TABLE III
GP OPTIMIZED RESULTS AND SPECTRERF SIMULATED PERFORMANCE

Performance	Specification	GP Achieved	Simulated
S_{11}	≤ -10dB	-19dB	-13.25dB
$Gain$	≥ 20dB	20dB	21dB
S_{22}	≤ -10dB	-21dB	-11dB
NF	≤ 2dB	1.61dB	1.84dB
IIP3	≥ -5dBm	-2.9dBm	-3.6dBm
Power	≤ 12.5mW	12.5mW	12.5mW

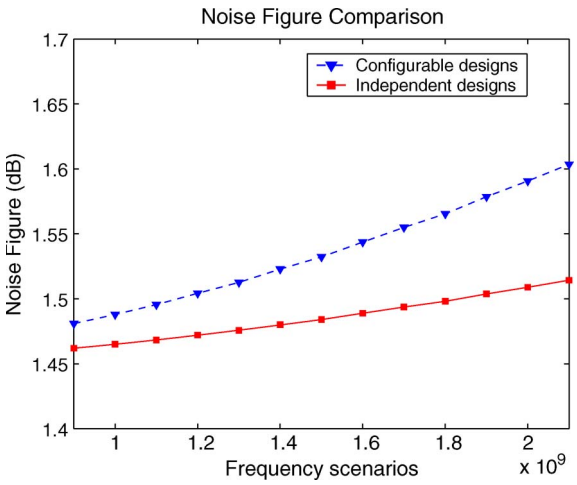

Fig. 6. Noise performance comparison.

The simulation results are also shown in Table III. We used Cadence's SpectreRF as the simulator with advanced device models. We conclude that GP optimization results and simulation results have good agreement with each other.

b) Center frequency configurable designs: Next, we describe a mask configurable SiGe LNA design at 13 different center frequencies, ranging from 900 MHz to 2.1 GHz with separation of 200 MHz. Other specifications are the same as listed in Table III. We use the average noise figure of all mask configurable designs as the cost function. The resulting problem has 96 variables and 364 constraints. The optimization process generates 13 metal-mask configurable designs with the same first-stage design results and 13 sets of second-stage design results.

Independent designs are obtained for each scenario as comparison. We compare the achieved noise figure for independent designs and configurable designs, as shown in Fig. 6. We can see that the NF of configurable designs are very close to independent designs and the maximum NF surcharge is less than 0.1 dB.

Since the circuit performance of configurable designs is very close to independent designs, the only penalty we pay for such flexibility is the silicon area. This is inevitable because the area of the implementation fabric would be larger than the maximum of all independent designs. The extent of the area penalty is a tradeoff with the amount of design risk. For example, in an LNA, the inductor areas are quite dominant. Reserving a fixed area for all inductors is the lowest risk approach, but incurs the largest area penalty.

c) Power and gain configurable designs: As a second example, we vary the power and gain specifications and observe the design space tradeoffs for mask configurability. The center frequency is fixed at 5.25 GHz. The power spec varies from 12.5 to 20 mW by every 0.5 mW, while the gain spec varies from 10 to 24 dB by every 2 dB. There are eight different gain requirements and 16 different power constraints. Therefore, in total we generate 128 design instances using the average NF of all designs as the cost function.

The achieved noise performance and NF surcharge of the mask configurable design are shown in Fig. 7. The plots show that the noise performance is more sensitive to power consumption. The NF surcharge of mask configurable design is less than 0.1 dB. In this way, design space exploration can be achieved in the early stages for the entire system design.

It is worth mentioning that the 128 designs with 901 variables and 3584 constraints are solved in 1.5 s, using the 1.4-GHz 256-MB memory Pentium PC.

6) Numerical Results of CMOS LNAs: We applied the same design methodology to a metal-mask configurable CMOS LNA design, using the CMOS devices in IBM 6HP BiCMOS technology. Some of the design equations for CMOS LNA design are summarized in [45].

In this example, instead of minimizing expected objective as cost function, we minimize the maximum design surcharge as defined in Section IV-C, which in this example is the difference between NF obtained in independent designs and NF obtained in configurable designs. We optimized a configurable design at nine different center frequencies, ranging from 1.5 to 5.5 GHz with separation of 500 MHz. The optimization generates nine design instances, as shown in Fig. 8. This example demonstrates that by using design surcharge as cost function, configurable designs can achieve performance very close to independent designs, with only area penalties.

B. Robust Oscillator Design Examples

To consider design variability in the early stages of design exploration in the ORACLE methodology, robust GP formulation is used to provide guaranteed yield bound. The following two examples show the robust optimization of RF oscillators.

1) Robust Optimization of an RO: The first example we will show is the robust optimization of an RO. The specific RO topology we consider in this paper is shown in Fig. 9. This is a widely used building block to characterize process variations. The performance and design variable relation has been extensively studied in [30]–[32].

To simplify the robust GP formulation, we consider three design variables and three performance specifications for this RO design. The three design variables are the following: effective width $W_{\text{eff}} = W_n + W_p$, gate length $L = L_n = L_p$, and gate over drive ΔV. They are related to the sizing and biasing of the NMOS and PMOS transistors.

The RO was designed to achieve minimal dynamic power consumption for a certain center frequency. The phase noise performance should not be larger than a given specification. The optimization has the following form:

$$\begin{aligned} \text{minimize} \quad & Power(W_{\text{eff}}, L, \Delta V) \\ \text{subject to} \quad & PN(W_{\text{eff}}, L, \Delta V) \leq PN^{\max} \\ & f_{\text{resonant}}(W_{\text{eff}}, L, \Delta V) = f_0 \end{aligned} \tag{38}$$

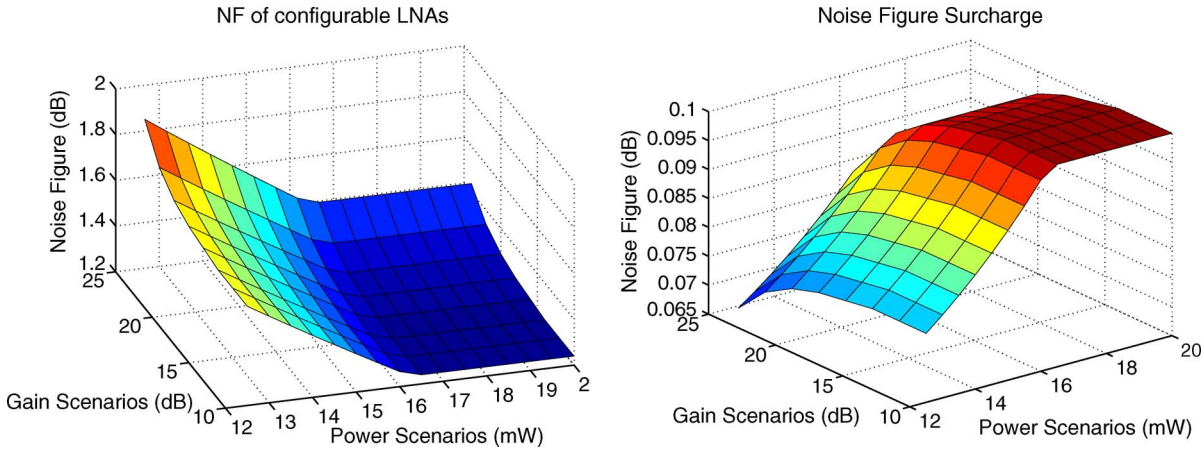

Fig. 7. NF of configurable LNAs and NF surcharges.

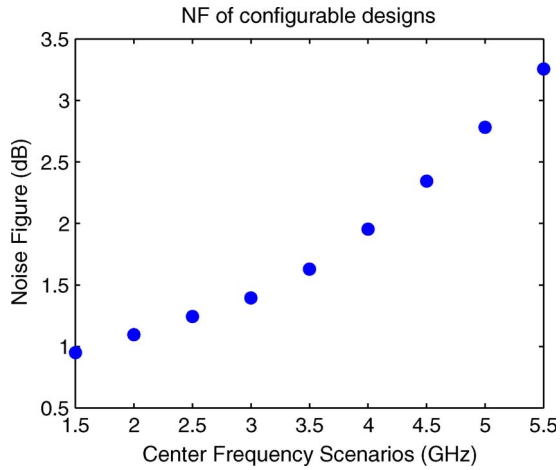

Fig. 8. CMOS LNA optimization results.

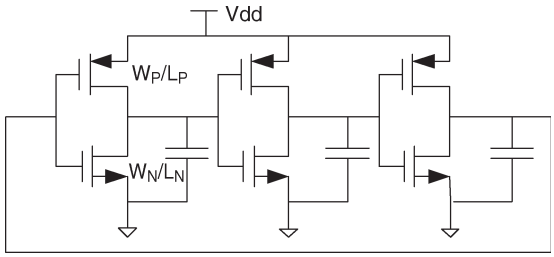

Fig. 9. Topology of an RO.

where f_0 is the given resonant center frequency and $PN^{\max}$ is the maximum phase noise specification.

In this example, we consider four variance-not-linked-to-mean, independent normal variations in process parameter and design variables. They are the gate width variation ΔW, the gate length variation ΔL, the gate oxide thickness variation $\Delta T_{\rm ox}$, and the threshold voltage variation $\Delta V_{\rm th}$. Here, the gate oxide thickness variation $\Delta T_{\rm ox}$ is reflected by coefficient perturbation in the GP of posynomial form [i.e., δp_i in (14)], and other three parameter variations are reflected by design variables perturbation [i.e., δx_i in (14)]. ($\Delta V_{\rm th}$ is considered as the gate overdrive voltage perturbation.) Then, the optimization (38) can be formulated as the GP of posynomial form considered in Section V-E2b, which can be further reformulated as the robust GP (6) to achieve the robust design with guaranteed yield bound.

TABLE IV
RO DESIGN RESULTS COMPARISON

Design Variables	GP achieved	robust GP achieved
Weff	$4.53\mu m$	$6.68\mu m$
Length	$0.26\mu m$	$0.24\mu m$
ΔV	0.42V	0.387V

TABLE V
RO PERFORMANCE MEAN COMPARISON

Performance Mean	GP achieved	robust GP achieved
Power	1.87mW	2.59mW
Phase Noise	-100dBc/Hz	-101dBc/Hz
Frequency	5GHz	4.85GHz

In the numerical example, we use the process parameter values extracted from the IBM 7HP 0.18-μm BiCMOS technology. The design is optimized when the confidence ellipsoid captures 90% of process variations, and the center frequency is relaxed within the interval [4 GHz, 6 GHz]. The design resulting from robust GP is compared with the design resulting from GP as listed in Table IV, and their performance means are listed in Table V.

The 10 K points Monte Carlo analysis is used to evaluate the performance variability and the parametric yield. The histogram of the phase noise performance of two designs resulting from GP and robust GP optimization are shown in Fig. 10. It can be concluded that the design using robust GP achieves higher yield with more design cost compared with nominal design using GP.

We further use the concentric ellipsoids $\mathcal{E}_\gamma$ (20) with various values of γ to capture different degrees of process variations. The tradeoff between the design cost and the yield bound is shown in Fig. 11, where the design cost (power consumption in this example) increases when higher yield bound is requested. It is also observed that a drastic increase in the design cost will be incurred to achieve yield close to 100%.

2) Robust Optimization of an LC Oscillator: The robust optimization and corner-based optimization are also compared using an LC oscillator example. The LC oscillator topology we consider in this paper is shown in Fig. 12. Five design variables and five performance specifications are considered for this LC

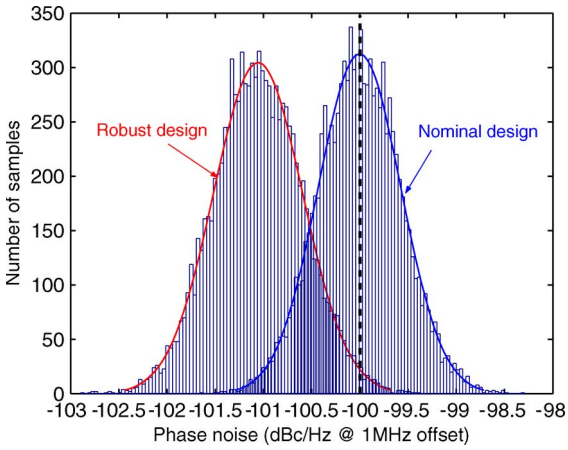

Fig. 10. Phase noise histogram comparison.

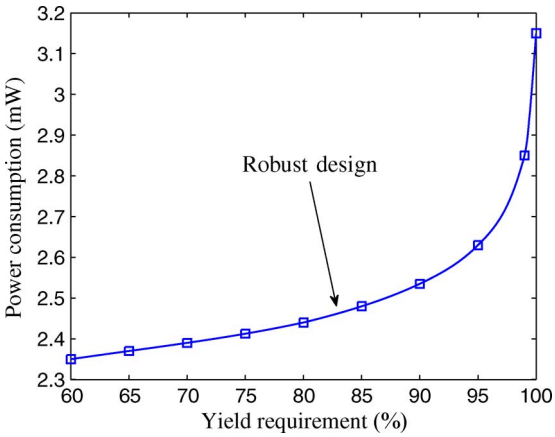

Fig. 11. RO design cost versus minimum yield spec.

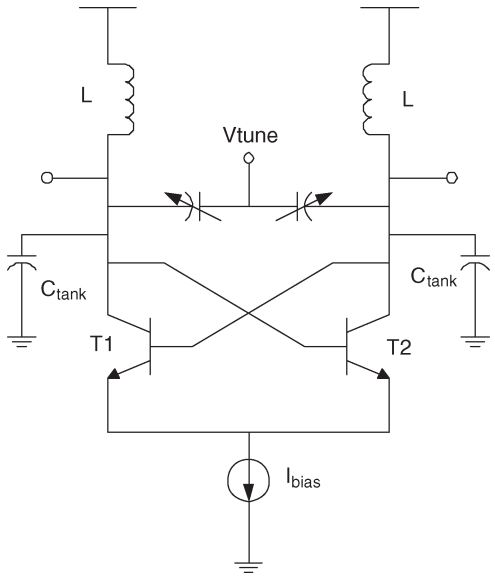

Fig. 12. Topology of an LC oscillator.

oscillator design. The five design variables are the following: the biasing tail current $I_{\rm bias}$, the lumped tank conductance $g_{\rm tank}$, the lumped tank capacitance $C_{\rm tank}$, the inductance L, and the output swing voltage $V_{\rm SW}$. They are key design variables in the lumped tank model.

TABLE VI
LC OSCILLATOR DESIGN RESULTS COMPARISON

	Robust optimization	Corner-based optimization
I_{bias}	2.41mA	2.72mA
C_{tank}	1.33pF	1.26pF
g_{tank}	0.894 mS	1.018 mS
L	2.83nH	2.82nH
V_{sw}	2.5V	2.5V

The LC oscillator was designed to achieve minimal dynamic power consumption for a certain center frequency [33]. The optimization has the following form:

$$\begin{aligned} \text{minimize} \quad & Power(I_{\rm bias}) \\ \text{subject to} \quad & PN(I_{\rm bias}, g_{\rm tank}, C_{\rm tank}, L, V_{\rm SW}) \le PN^{\max} \\ & f_{\rm resonant}(C_{\rm tank}, L) = f_0 \\ & LoopGain(I_{\rm bias}, g_{\rm tank}) \ge LG^{\min} \\ & V_{\rm SW} \le V_{\rm dd} \\ & V_{\rm SW} \le \frac{I_{\rm bias}}{g_{\rm tank}} \end{aligned} \tag{39}$$

where f_0 is the given resonant center frequency, $PN^{\max}$ is the maximum phase noise specification, $LG^{\min}$ is the minimum loop gain specification and $V_{\rm dd}$ is the power supply voltage.

In this example, we consider three variance-linked-to-mean correlated normal variations in process parameters. They are the relative tank conductance variation $\Delta g_{\rm tank}/g_{\rm tank}$, the relative tank capacitance variation $\Delta C_{\rm tank}/C_{\rm tank}$, and the relative inductance variation $\Delta L/L$. Then, the optimization (39) can be formulated as the GP of posynomial considered in Section V-E2a, which can be further reformulated as the robust GP (6) to achieve the robust design with guaranteed yield bound.

In the numerical example, we use the process parameter values extracted from Hitachi 90-GHz 0.25-μm BiCMOS technology. The design is optimized when the confidence ellipsoid capture 90% of process variations, and the center frequency is relaxed within the interval [1.7 GHz, 2.5 GHz]. Note that the process corners are provided by the foundry which reflect the vertices of the regular polyhedron where the ellipsoid used in the robust optimization is inscribed. We compare the robust optimization results with the corner-based optimization results as listed in Table VI.

We also use the concentric ellipsoids $\mathcal{E}_\gamma$ (17) with various values of γ to capture different degrees of process variations. The design costs (power consumption in this example) using two optimization schemes will increase when the yield requirement increases, as compared in Fig. 13. The actual yield of each design is found using 10 K points Monte Carlo analysis. The design cost versus actual yield for the two optimizations in compared in Fig. 14. It is shown in this example that about 20% overdesign is observed in the corner-based optimization compared to robust optimization when $\pm 3\sigma$ actual yield is achieved.

VII. CONCLUSION

Regular analog/RF IC using metal-mask configurability can be used to reduce design risk and manufacturing cost. In this paper, we proposed an ORACLE design methodology and the

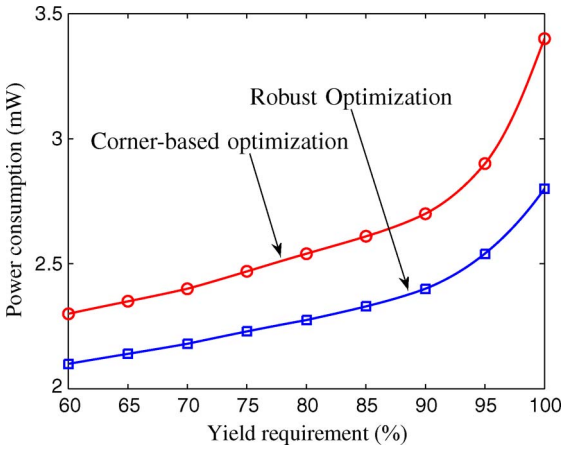

Fig. 13. *LC* oscillator design cost versus minimum yield spec.

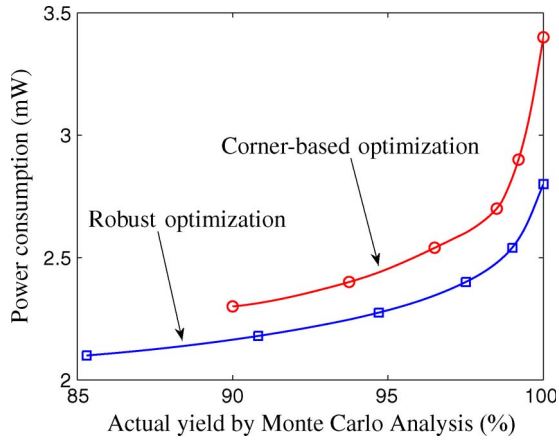

Fig. 14. *LC* oscillator design cost versus actual parametric yield.

enhanced robust optimization feature for such regular integrated circuits. Our methodology and optimization procedure is applied in a set of metal-mask configurable LNA designs and the robust optimization of RF oscillators. Numerical examples demonstrate that competitive performance can be achieved with guaranteed yield. The regular design and supporting methodology are used in the silicon implementation of three RF front-end circuits in a 0.25-μm 1P6M SiGe BiCMOS process. The measured results demonstrated the validity of such optimization framework [9].

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