

# Shuvendu K. Lahiri

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CONTACT INFORMATION	Hamerschlag Hall 2132 Electrical and Computer Engineering Department Carnegie Mellon University Pittsburgh, PA 15213 USA	<i>Voice:</i> (412) 247-7454 <i>Fax:</i> (412) 268-3336 <i>E-mail:</i> shuvendu@ece.cmu.edu <i>WWW:</i> www.ece.cmu.edu/~shuvendu
STATUS	<i>Citizenship:</i> Indian	<i>Visa:</i> F1
RESEARCH INTERESTS	Decision Procedures for first-order logic, formal verification of distributed unbounded systems, invariant synthesis, predicate abstraction, microprocessor verification.	
OBJECTIVE	Obtain a position in formal verification or decision procedure research in academia or research laboratories.	
EDUCATION	<b>Carnegie Mellon University, Pittsburgh, Pennsylvania USA</b> Ph.D., Computer Engineering, (expected: August 2004) <ul style="list-style-type: none"><li>• Dissertation Topic: "Efficient techniques for Unbounded System Verification"</li><li>• Advisor: Prof. Randal E. Bryant</li><li>• GPA: 3.99/4.00</li></ul> M.S., Computer Engineering, May 2001 <ul style="list-style-type: none"><li>• Dissertation Topic: "An efficient decision procedure for the logic of Counters, Constrained Lambda expressions, Uninterpreted Functions and Ordering"</li><li>• Advisor: Prof. Randal E. Bryant</li><li>• GPA: 4.00/4.00</li><li>• Relevant Graduate Courses: Specification and Verification, Separation Logic, Automated Theorem Proving, Verification of Concurrent and Reactive Systems, Advanced AI techniques, Mathematical Logic (I, II), Type theory for programming languages.</li></ul> <b>Indian Institute of Technology, Kharagpur, India</b> B.Tech., Computer Science and Engineering, May, 1999 <ul style="list-style-type: none"><li>• Dissertation Topic: "Symbolic and Automata-Theoretic Model Checking for Timed Abstraction of Verilog Descriptions"</li><li>• Advisor: Prof. P. P. Chakrabarti and Prof. P. Dasgupta</li><li>• GPA: 9.4/10.0</li><li>• Ranked 6th (out of about 500) students in the entire batch.</li></ul>	
ACADEMIC EXPERIENCE	<b>Carnegie Mellon University, Pittsburgh, Pennsylvania USA</b> <i>Graduate Student</i> Worked on modeling and verifying systems with unbounded resources. Developed the logic of CLU and efficient decision procedures for the logic, symbolic techniques for performing predicate abstraction efficiently and extended predicate abstraction to deal with systems with unbounded data structures. Investigated model checking of systems with unbounded resources. All these ideas have been integrated into a tool UCLID ( <a href="http://www.cs.cmu.edu/~uclid">www.cs.cmu.edu/~uclid</a> ), a verifier for infinite-state systems.  <i>Teaching Assistant</i> Undergraduate course on "Introduction to Real-Time Embedded Systems".  <i>Teaching Assistant</i> Graduate course on "Hardware Systems Engineering"	<b>Aug 1999 – present</b>  <b>Aug 2002 – Dec 2002</b>  <b>Jan 2002 – May 2002</b>

PROFESSIONAL  
EXPERIENCE

**Software Productivity Tools**, Microsoft Research, Redmond, USA.

*Research Intern*

**June 2003 – Sept 2003**

Worked on various symbolic reasoning tools inside the software verification tool SLAM. Designed and implemented a lazy proof-generating SAT-based theorem prover ZAPATO for quantifier-free fragment of first-order logic. Also worked on a fast but approximate predicate abstraction scheme for software verification.

**Advanced Tools Group**, Motorola, Austin, USA

*Summer Intern*

**May 2001 – Aug 2001**

The main focus was to derive a term-level model of a variant of PowerPC™ microprocessor. The tool UCLID was used to perform symbolic simulation on the high-level model.

*Summer Intern*

**May 2000 – Aug 2000**

Extracted a term-level model of the Motorola M\*CORE embedded processor. The tool CMU-EVC was used to verify the model by using Burch-Dill verification technique. The project discovered four critical bugs in the datapath even before the deployment of the actual Verilog. This was one of the first success stories of high-level design verification in the microprocessor industry.

**Research and Development Group**, Synopsys, Bangalore, India

*Summer Intern*

**May 1998 – July 1998**

Worked on improving the performance of *static simulation* of Verilog code. Also worked on testing and debugging the VCS simulator.

PUBLICATIONS

“Controlling State Explosion in Static Simulation by Selective Composition” P.P.Chakrabarti, Pallab Dasgupta, P.P.Das, Arnob Roy, Shuvendu Lahiri, and Mrinal Bose. In *12th International Conference on VLSI DESIGN '99*.

“Experience with Term-level modeling and verification of Motorola M\*CORE microprocessor core”, Shuvendu K. Lahiri, Carl Pixley, Ken Albin. In *Proc. IEEE High Level Design Validation and Test (HLDVT) Workshop, Nov 2001*.

“Modeling and Verifying Systems using a Logic of Counter Arithmetic with Lambda Expressions and Uninterpreted Functions”, Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia. In *Proc. of Computer-Aided Verification (CAV), July 2002*.

“Deciding CLU Logic Formulas via Boolean and Pseudo-Boolean Encodings”, Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia. In *Proc. Intl. Workshop on Constraints in Formal Verification, September 2002*. Associated with Intl. Conf. on Principles and Practice of Constraint Programming.

“Modeling and Verification of Out-of-order Microprocessors in UCLID”, Shuvendu K. Lahiri, Sanjit A. Seshia, and Randal E. Bryant. In *Proc. Intl. Conf. on Formal Methods in Computer-Aided Design (FMCAD), November 2002*.

“A Hybrid SAT-based Decision Procedure for Separation Logic with Uninterpreted Functions”, Sanjit A. Seshia, Shuvendu K. Lahiri, Randal E. Bryant. In *Proc. Design Automation Conference (DAC), June 2003*.

“Deductive Verification of Advanced Out-of-Order Microprocessors”, Shuvendu K. Lahiri and Randal E. Bryant. In *Proc. of Computer-Aided Verification (CAV), July 2003*.

“A Symbolic Approach to Predicate Abstraction”, Shuvendu K. Lahiri, Randal E. Bryant and Byron Cook. In *Proc. of Computer-Aided Verification (CAV), July 2003*.

“Convergence Testing in Term-level Bounded Model Checking” Randal E. Bryant, Shuvendu K. Lahiri and Sanjit A. Seshia. In *Proc. of 12th Conference on Correct Hardware Design and Verification Methods (CHARME), October 2003*.

“Constructing Quantified Invariants via Predicate Abstraction” Shuvendu K. Lahiri and Randal E. Bryant. In *Proc. of 5th Intl. Conference on Verification, Model Checking and Abstract Interpretation (VMCAI), January 2004*

“Revisiting Positive Equality” Shuvendu K. Lahiri, Randal E. Bryant, Amit Goel and Muralidhar Talupur. In *Proc. of 10th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), March 2004*

“Indexed Predicate Discovery for Unbounded System Verification”, Shuvendu K. Lahiri, Randal E. Bryant. In *Computer-Aided Verification (CAV), 2004*.

“The UCLID Decision Procedure”, Shuvendu K. Lahiri, Sanjit A. Seshia. In *Computer-Aided Verification (CAV), 2004* (Tool description).

“Zapato: Automatic Theorem Proving for Software Predicate Abstraction Refinement”, Thomas Ball, Byron Cook, Shuvendu K. Lahiri, Lintao Zhang. In *Computer-Aided Verification (CAV), 2004* (Tool description).

PAPERS IN  
PREPARATION

“Symbolic and Indexed Predicate Abstraction”, Shuvendu K. Lahiri and Randal E. Bryant. To be submitted to *ACM Transactions on Computational Logic*.

“Modeling and Verification of Complex Out-of-Order Microprocessors in UCLID”, Shuvendu K. Lahiri and Randal E. Bryant. To be submitted to *Formal Methods in System Design*.

“Fast Predicate Abstraction for Software Verification”, Thomas Ball, Byron Cook, Shuvendu K. Lahiri, Sri-ram K. Rajamani. In *preparation*.

REVIEWER

JAR, FSTTCS, CAV, CHARME, POPL, FMCAD, IWLS, DATE, SoftMC,TECS

HONORS AND  
AWARDS

Semiconductor Research Corporation (SRC) Scholarship, 1999 – present  
Motorola award for one of the outstanding interns, 2000  
Stood first in class X (1993) and XII (1995) in high school

INVITED  
PRESENTATIONS

*Unbounded System Verification using Predicate Abstraction*. Computer Science Department, Courant School of Mathematical Sciences, New York University, March 2004.

*A Symbolic Approach to Predicate Abstraction*. Synopsys Inc., Beaverton, July 2003.

*The UCLID Verification System*. Guest Lecture, Graduate Course, Hardware Systems Engineering (18-744), CMU, Spring 2003, Spring 2004.

*UCLID: Deciding Combinations of Theories via Eager Translation to SAT*. Combination of Decision Procedures Summer School, SRI International, Menlo Park, USA, August 9 – 11, 2004. This was a two-part talk given jointly with Sanjit A. Seshia.

COMPUTER SKILLS

- Operating Systems: Unix/Linux, Windows.
- Languages: C/C++, Java, SML/OCAML/MOSML, Lex, Yacc, Perl, Verilog

REFERENCES

- Prof. Randal E. Bryant, School of Computer Science, Carnegie Mellon University.  
Email: Randy.Bryant@cs.cmu.edu
- Prof. Edmund M. Clarke, School of Computer Science, Carnegie Mellon University.  
Email: emc@cs.cmu.edu

- Dr. Carl Pixley, Advanced Technology Group, Synopsys Inc.  
Email: cpixley@synopsys.COM
- Dr. Thomas Ball, Testing, Verification and Measurement, Microsoft Research.  
Email: tball@microsoft.com
- Prof. P. P. Chakrabarti, Computer Science and Engineering,  
Indian Institute of Technology, Kharagpur, India.  
Email: ppchak@cse.iitkgp.ernet.in