

# Sounil Biswas

CONTACT INFORMATION 5625 Hempstead Road  
Apt 204  
Pittsburgh, PA 15217 USA

Phone: (412) 445-5396  
E-mail: [sbiswas@ece.cmu.edu](mailto:sbiswas@ece.cmu.edu)  
WWW: <http://www.ece.cmu.edu/~sbiswas>

OBJECTIVE Seeking a challenging career in the field of Integrated Systems design and test to develop industry-leading solutions for optimizing manufacturing cost and improving product quality and reliability.

AREA OF EXPERTISE

- Design, Test and Diagnosis of Integrated Systems
- Statistical analysis of performance specifications – Manufacturing and Test Strategy development
- Failure analysis and Defect characterization
- Quality and Reliability analysis
- 6+ years of software tool development using C/C++ and other high level programming languages

SKILLS

- **Test and Timing Tools:** Cadence Encounter Test/TestBench, Synopsys Primitime, Atalanta, HOPE
- **Mathematical/Statistical Packages:** SAS JMP, MATLAB, R, SVM<sup>light</sup>
- **Programming Languages:** C/C++ (over 50K lines of code), Perl, MATLAB, Cadence SKILL/OCEAN, Lex/Yacc, Shell Scripts (Bash, Csh)
- **Program Debuggers:** GDB/DDD, Valgrind, IBM Rational PurifyPlus
- **Simulation Software:** Synopsys HSPICE, Verilog, VHDL, Berkeley SIS/BLIF
- **Design/Layout Software:** Cadence Spectre (VerilogA), Cadence Virtuoso, Cadence Silicon Ensemble, Magic
- **Platform/OS:** Linux (Redhat/Suse), Unix (Solaris, AIX), MS Windows (NT/2000/XP/Vista)
- **Applications:** LaTeX, Microsoft Office, Open Office/Star Office, Adobe FrameMaker, Visual Studio, Emacs/Xemacs
- **Foreign Languages:** Spanish

ACADEMIC BACKGROUND

**Carnegie Mellon University**, Pittsburgh, PA

Ph.D. – Electrical & Computer Engineering **expected February 2008**

- Thesis: “Statistical Test Compaction in Integrated, Heterogeneous Systems”

M.S. – Electrical & Computer Engineering **May 2004**

- Thesis: “A Comprehensive Method for Generalized Sensitization and Test Control Using Fault Tuples”

**Indian Institute of Technology (IIT), Kanpur**, India

B.Tech (Hons.) – Electrical Engineering **May 2002**

- Thesis: “A Path Sensitization Technique for Testing Switched Capacitor Circuits”

RESEARCH EXPERIENCE

**Carnegie Mellon University** **August 2002 – Present**

*Research Assistant, Center for Silicon Systems Implementation (CSSI)*

- Developing a statistical test compaction methodology where redundant tests are identified and eliminated from specification based test set in an integrated heterogeneous system (*i.e.*, mixed-signal, analog, micro-systems, *etc.*).
- Proposed new 5-value algebra and new path sensitization scheme, which were used to develop robust and hazard-free tests for arbitrary logical faults over any number of clock cycles in a digital circuit.
- Collaborating with an off-site team of engineers at **Freescale Semiconductors** to analyze the possible elimination of low and high temperature vibration tests for a commercial sensor. Findings were presented on multiple occasions.
- Collaborating weekly with two of-site teams at **IBM Microelectronics** to identify possible redundant tests in a commercial PLL (Phase Locked Loop) and a commercial high speed SERDES (Serializer/Deserializer) circuit. Weekly status presented to the IBM teams via teleconferencing.
- Collaborating with an off-site RF design group at **IBM Microelectronics** to eliminate part or all of the high frequency RF tests for a commercial mobile phone chip.
- Acting as project mentor for multiple graduate students from June 2007 to present date.
- Proficient in working together with cross-site work groups.

*Senior Year Research, VLSI Laboratories*

- Developed a novel test methodology for the sensitization of charge transfer paths in Switched Capacitor (SC) circuits.

**PROJECTS****Placement and Routing tools**

- C++ implementation of a Timing-driven Quadratic Placement tool that optimized the Elmore delays of critical paths for a given set of industry designs.
- C++ implementation of a Maze Routing tool – global and detailed routing of various industry designs minimizing wire congestion as well as wire lengths.

**Circuit Simulation tool**

- MATLAB-based DC and transient analysis tool for linear and PWL (Piecewise Linear) circuits. Techniques used – Reduced order moment matching (AWE and PRIMA), Newton-Rhapson analysis.

**ATPG (Automatic Test Pattern Generation) and Fault Simulation**

- C/C++ implementation of PODEM and FAN-based ATPG tool – used to generate test patterns that detect 100% of the SSL (Single Stuck Line) faults for ISCAS'89 and ITC'99 benchmark circuits.
- C/C++ implementation of a Concurrent Fault Simulator – used to determine the detected SSL and bridging faults for the same circuits with a given set of test patterns.

**DFT (Design for Test)**

- Full Scan, Boundary Scan and BIST (Built-In Self Test) – Optimized chip area, power and pin count.

**Semiconductor IC Fabrication**

- Starting from Silicon Wafers to Chip Dicing and Probe Testing. Experience with process steps Spin-on-Glass, Aluminum Sputtering, Photolithography, Wet Etching, DRIE (Deep Reactive Ion Etching), *etc.*

**DFM/DFY (Design for Manufacturability/Yield)**

- Manufacturability improvement through OPC (Optical Proximity Correction) for a 3×3 SRAM – modified GDSII layout by adding hammer-heads, resizing layouts, adding dummy structures, *etc.*
- Yield analysis using estimated probabilities of occurrences of Spot Defects of varying radii using Critical Area calculations. Dummy rows and columns were added to analyze the yield improvements.

**Circuit Design**

- Designed a 2.5 GHz Clock and Data Recovery Circuit using CMOS and Differential logic.
- Worked in a three person team to divide the task, collaborate and reach the final design.

**Human Language Translation Device – LinguiStick<sup>®</sup>**

- Design, Financial/Market analysis and Product Launch Strategy of the device. The device has been submitted by course instructor to a lawyer and is being considered for filing a patent.

**OTHER****Transwitch Inc. and Ecole Polytechnique Federale Lausanne (EPFL)****EXPERIENCE***Intern***May 2001 – July 2001**

Design of a 10/100Mbps (extendable to a 1Gbps) MAC (Media Access Control) layer for an IP Core.

**Carnegie Mellon University***Teaching Assistant***August 2007 – December 2007, August 2005 – December 2005**

- Graduate level class on Digital Systems Testing and Testable Designs.

**REFEREED****PUBLICATIONS**

- S. Biswas and R. D. (Shawn) Blanton, “Statistical Test Compaction using Binary Decision Trees,” *IEEE Design & Test of Computers: Special Issue on Process Variation and Stochastic Design and Test*, vol. 23, no. 6, pp. 452 – 462, Jun. 2006.
- S. Biswas, P. Li, R. D. (Shawn) Blanton and L. T. Pileggi, “Specification Test Compaction for Analog Circuits and MEMS,” *Proc. of Design, Automation and Test Conf. in Europe*, pp. 164 – 169, Mar. 2005.
- S. Biswas, K. N. Dwarakanath and R. D. (Shawn) Blanton, “Generalized Sensitization using Fault Tuples,” *Proc. of VLSI Test Symp.*, pp. 297 – 303, Apr. 2004.
- S. Biswas and B. Mazhari, “A Path Sensitization for Testing Switched Capacitor Circuits,” *Proc. of Intl. Conf. on VLSI Design*, pp. 30 – 35, Jan. 2003.

**HONORS AND****AWARDS****Carnegie Mellon University – Graduate Fellowship****August 2002 – Present****IIT, Kanpur – Shridhar Memorial Prize for Best Student****1998 – 2001**