

ECE 18-766: Art & Science of System-Level Design¹

COURSE DESCRIPTION

The objective of this course is to present the necessary background, useful abstractions and needed techniques for system-level modeling, analysis and optimization. The course is primarily intended to provide the fundamentals on using concurrency theory concepts to represent and evaluate the behavior of different embedded applications. These include choosing the appropriate modeling formalism, constructing, solving and optimizing the model, and finally make the appropriate design decisions towards an efficient practical implementation. While the emphasis is on both computation and communication aspects involved in the Systems-On-a-Chip design of embedded applications, parts of the course will also cover modern topics related to nanotechnologies, ambient intelligence and systems biology. The main idea is to illustrate the beauty and the power of the system-level approach at work for a variety of practical systems.

Roughly speaking, the course tries to present the basics of SOC design methodologies, review hot topics in the design of embedded systems and identify promising directions for future research. By structure and contents, this class is targeted primarily towards computer engineers with research interests in the design and performance evaluation of modern embedded systems. It may also provide a valuable basis for students in computer science and related subjects.

Topics to be covered include: models of concurrency, specification & modeling of embedded applications, communication-based design, self-similarity and criticality issues, on-chip networks, low-power & reliable design, design paradigms for nanotechnologies, ambient intelligence, systems biology. The course requirements consist of a few homework assignments, a semester-long project, and class presentations based on relevant papers and students work on the project.

CLASS INFORMATION

Time/Place Mon/Wed 2:30 - 4:20PM (lectures) PH A18A
Tue 4:30 - 6:20PM (mandatory discussion sessions) HH B131

Web page <http://www.cmu.edu/blackboard>

Instructor Radu Marculescu, office HH 2108, tel. x8-8710, email radum@ece.cmu.edu
Office hours: Mon/Wed 4:30PM - 5:30PM

TA Umit Ogras, office HH 2131, tel. x8-5234, email uogras@andrew.cmu.edu
Office hours: Tue 2:00PM - 4:00PM

Secretary Judy Bandola, office HH 2107, tel. x8-2224, email judy@ece.cmu.edu

TEXTBOOK

None. A collection of relevant papers to system-level design of embedded applications will be used.

1. Also known as "Formal Methods for SOC Design". This syllabus may be revised during the term.

EXPECTED WORK

Assignments	Description	% of final grade	Obs
3 HWs	The homework assignments will be based on the material discussed in the class, as well as some research papers. The HWs may involve work with Matlab (Stateflow) and other software.	30%	HWs are due at the beginning of the class. No late HWs will be accepted.
Paper presentations & in-class discussions	Relevant papers will be assigned to students for review and in class presentation. The quality of presentation and the participation in the related discussions are part of the grade.	20%	10% Presentation+Q&A 10% Participation
Project	A few projects (which may involve original contribution!) will be proposed by the instructor. Students are also encouraged to propose new topics based on their own research interests or the material discussed in the class. Work in teams of 2 people is strongly suggested but not strictly enforced. In addition, each team will be required to present and demo their project to the entire class. At the end, all contributions will be collected in a single edited volume which will be distributed to all registered students in the class. A best project ward will be given.	50%	10% Proposal 10% Milestone 1 10% Milestone 2 20% Final Any project proposal or report can be submitted up to 5 days late, but it will be subject to a 10% per day late penalty. The 10% penalty is computed based on the <i>maximum</i> number of points, not on your actual achieved score. No other extensions will be given.

WHAT 18-766 IS ABOUT

A natural bridge between EE and CS concepts. Mostly research-oriented, interdisciplinary, with strong emphasis towards formal approaches. Meant to discover the beauty of doing independent research and working in a team to get the job done. An attempt to reduce the gap between grad school education and real life competition.

WHAT 18-766 IS NOT

A class where you only use CAD tools to design circuits or do layout. A class which does not involve thinking, independent work, and original contribution. Finally, a class where you'll learn everything about SOC design and get answers to all your questions.

BOOKS (recommended, NOT required)

Communication & Concurrency/by Robin Milner, Prentice Hall, 1989.

Concurrency: State models and Java programs/by Jeff Magee and Jeff Kramer, Wiley, 1999.

Operating Systems Concepts/by Silberchatz and Galvin, Wiley 2001.

Networks on Chip, A. Jantsch and Hannu Tenhunen (eds.) Kluwer Academic Publishers, 2003.

Power Aware Design Methodologies, Massoud Pedram, Jan M. Rabaey (eds.), Kluwer Academic Publishers, 2002.