

Page Overlays

An Enhanced Virtual Memory Framework to
Enable Fine-grained Memory Management

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Onur Mutlu, Phillip B. Gibbons, Michael A. Kozuch,
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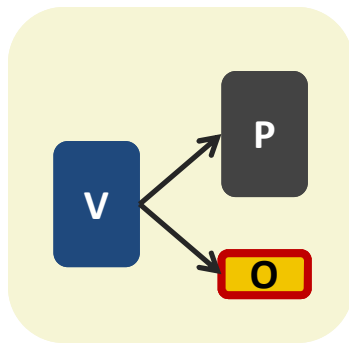
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Research

Executive Summary

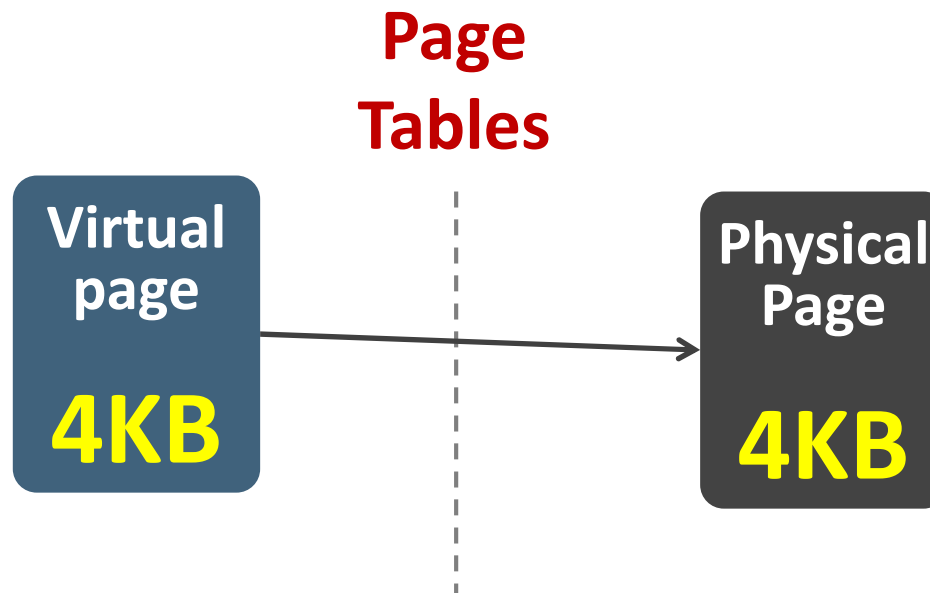
- Sub-page memory management has several applications
 - More efficient capacity management, protection, metadata, ...
- Page-granularity virtual memory → inefficient implementations
 - Low performance and high memory redundancy



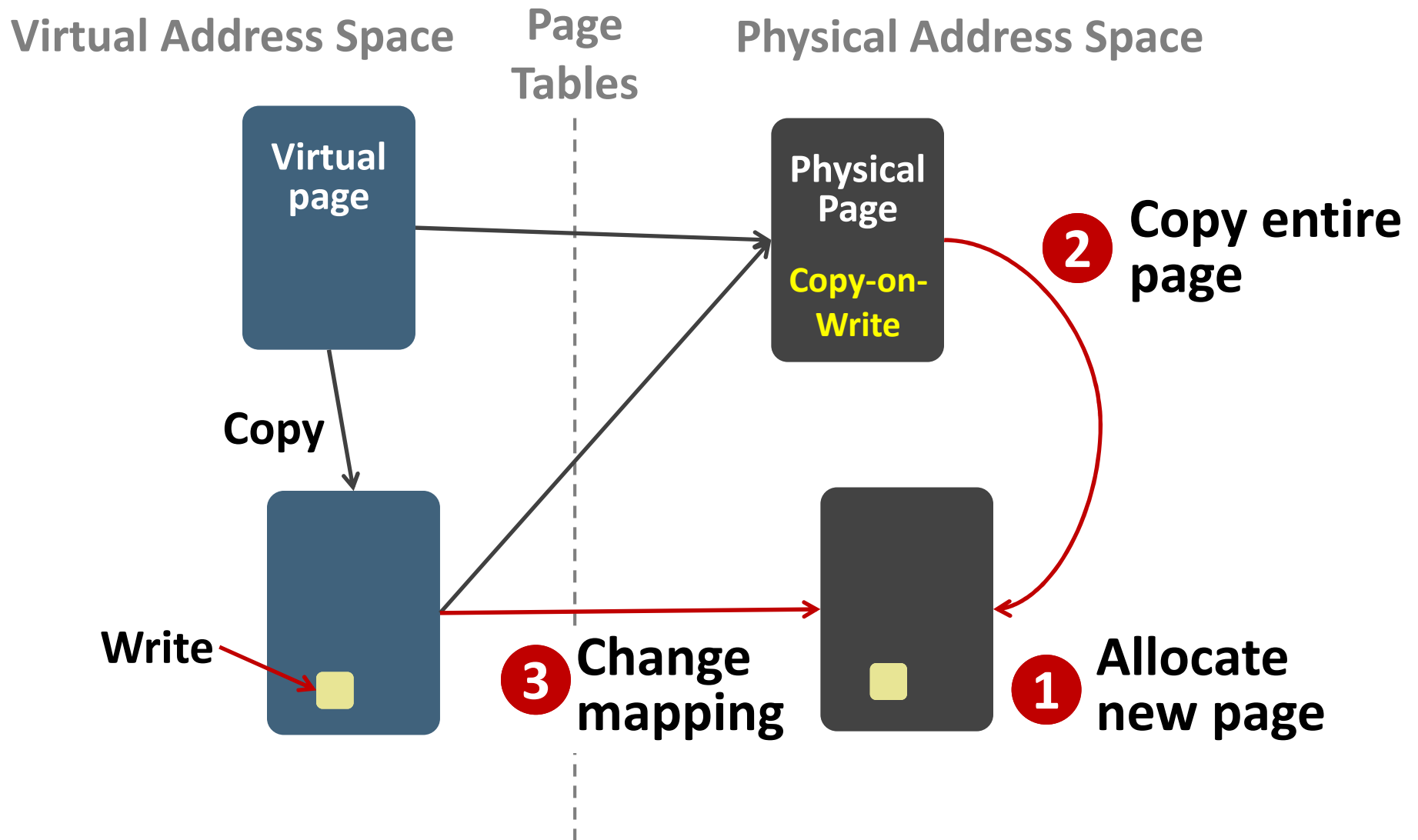
- **Page Overlays: New Virtual Memory Framework**
- Virtual Page → (physical page, **overlay**)
 - Overlay contains new versions of subset of cache lines
 - Efficiently store pages with mostly similar data
- **Largely retains existing virtual memory structure**
 - Low cost implementation over existing frameworks
- **Powerful access semantics – Enables many applications**
 - E.g., overlay-on-write, efficient sparse data structure representation
- Improves performance and reduces memory redundancy

Existing Virtual Memory Systems

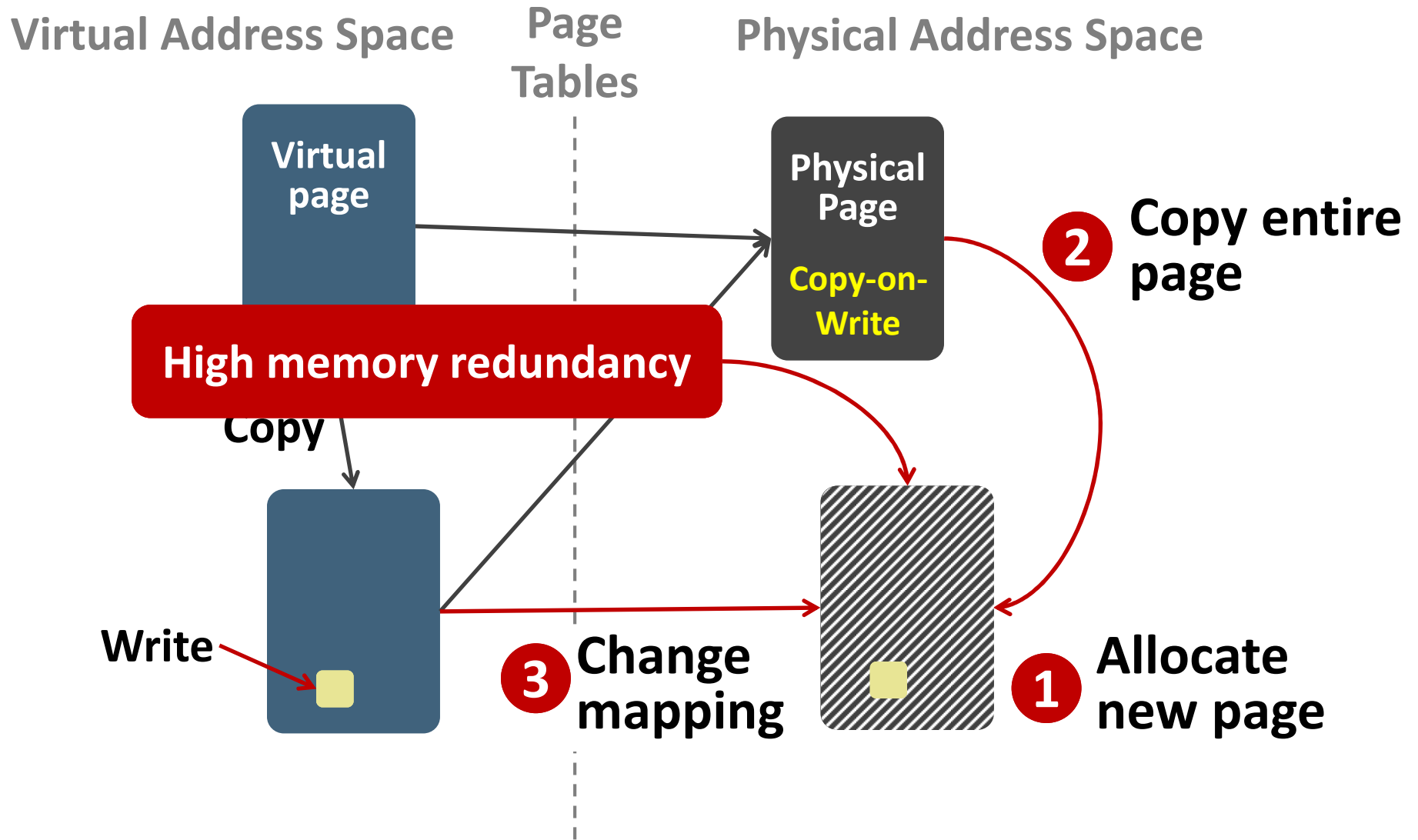
- Virtual memory enables many OS functionalities
 - Flexible capacity management
 - Inter-process data protection, sharing
 - Copy-on-write, page flipping



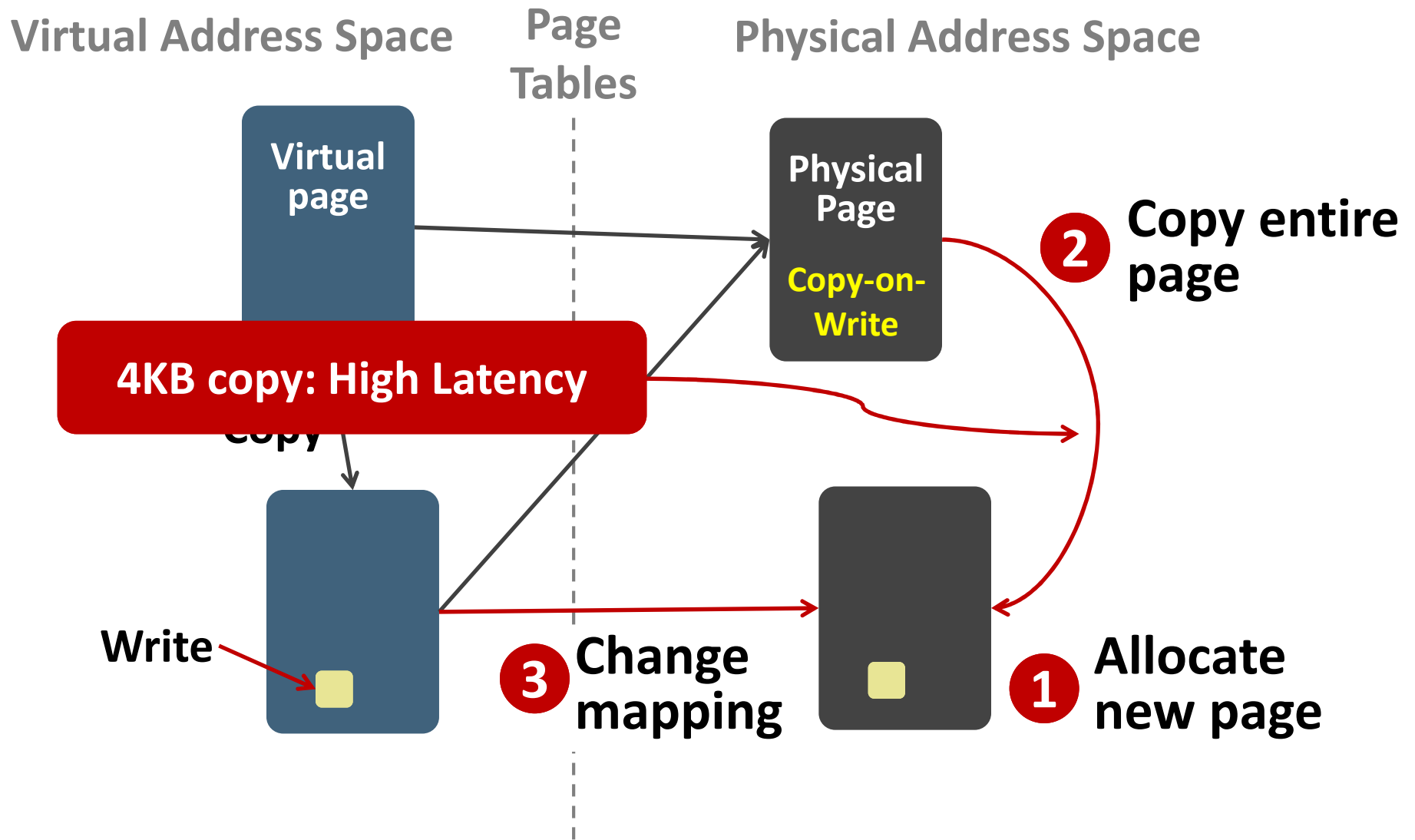
Case Study: Copy-on-Write



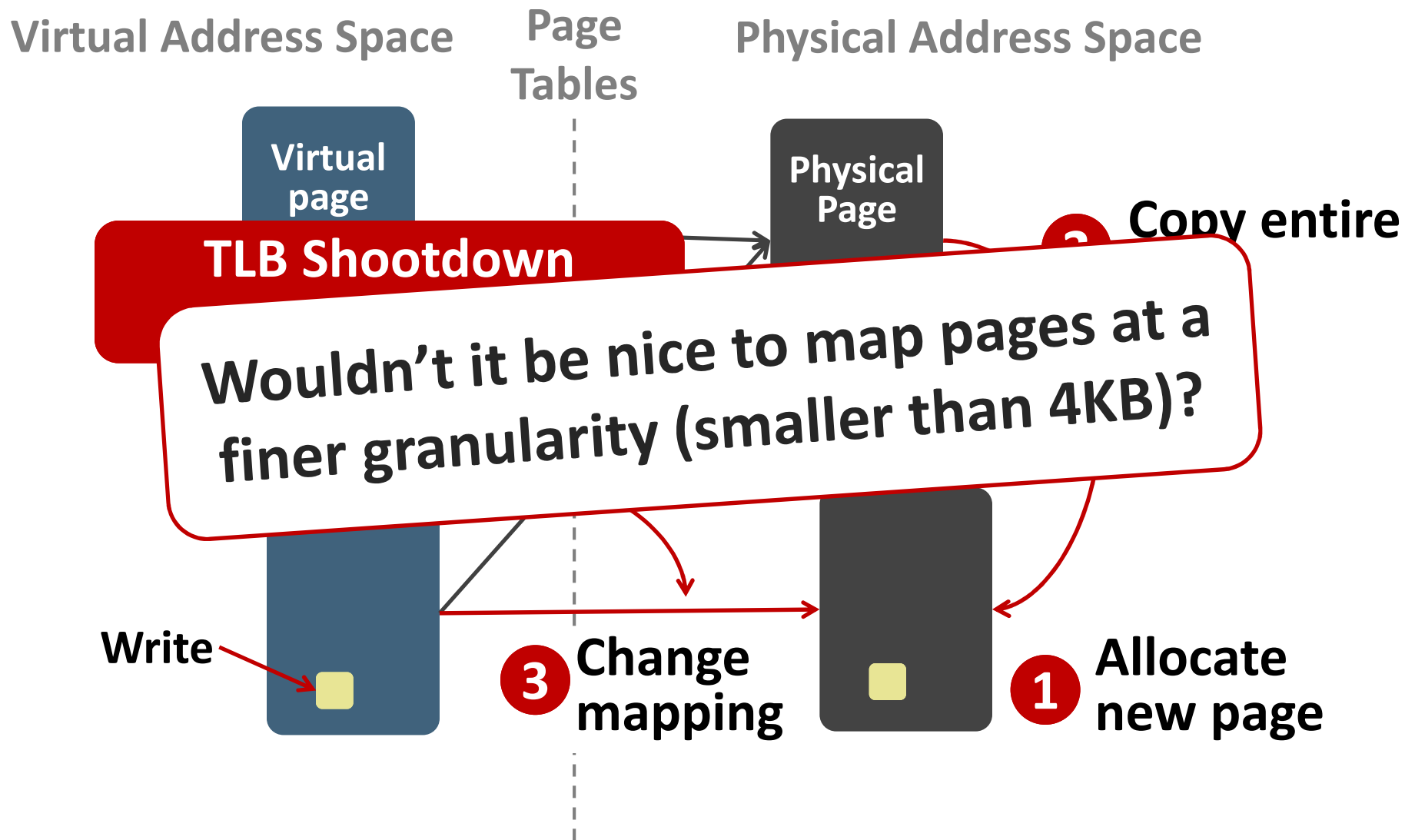
Shortcomings of Page-granularity Management



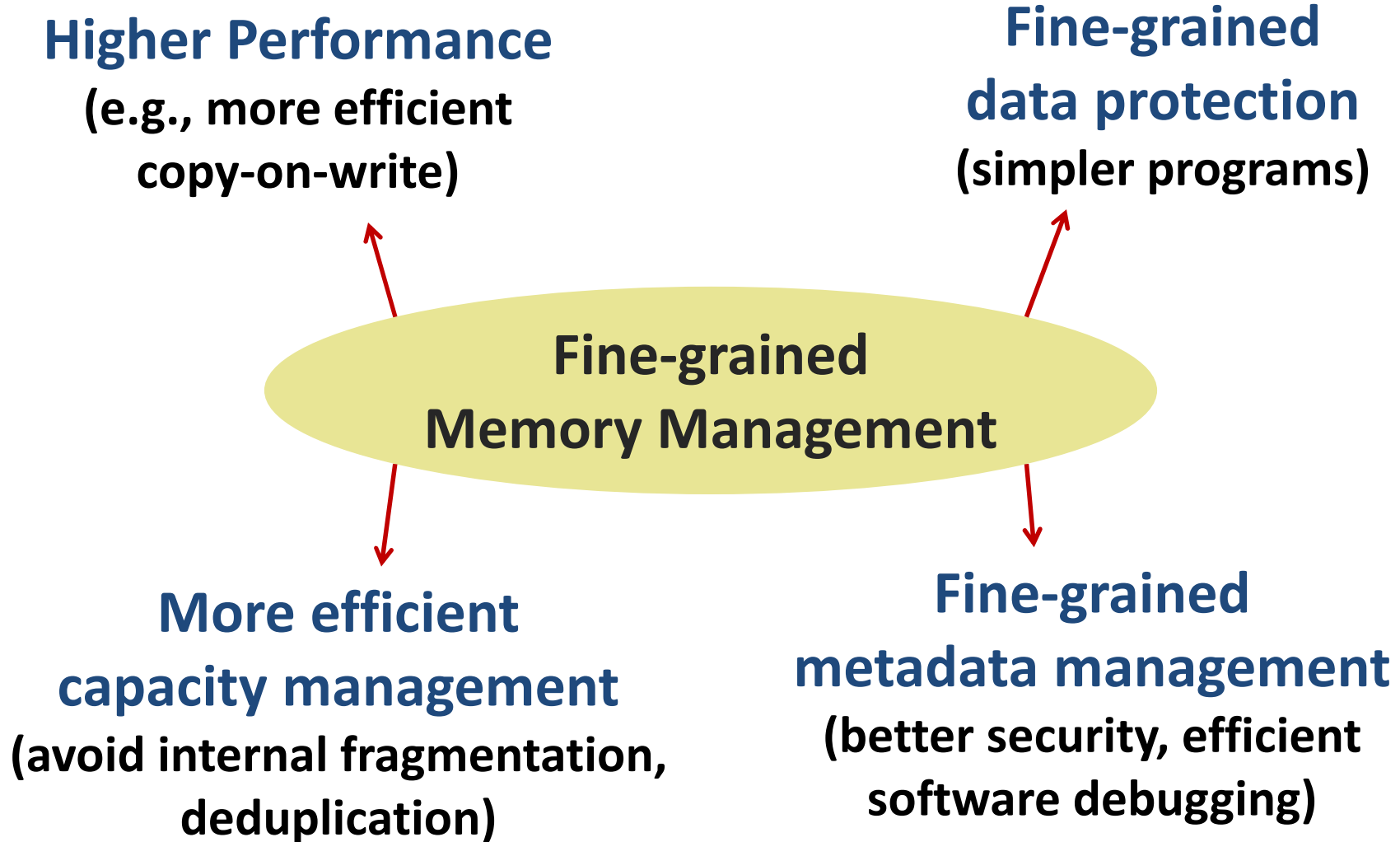
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Shortcomings of Page-granularity Management

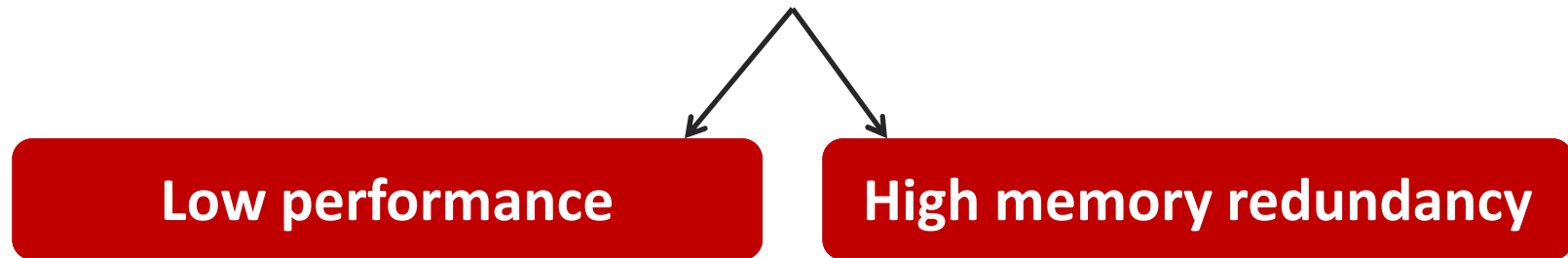


Fine-grained Memory Management

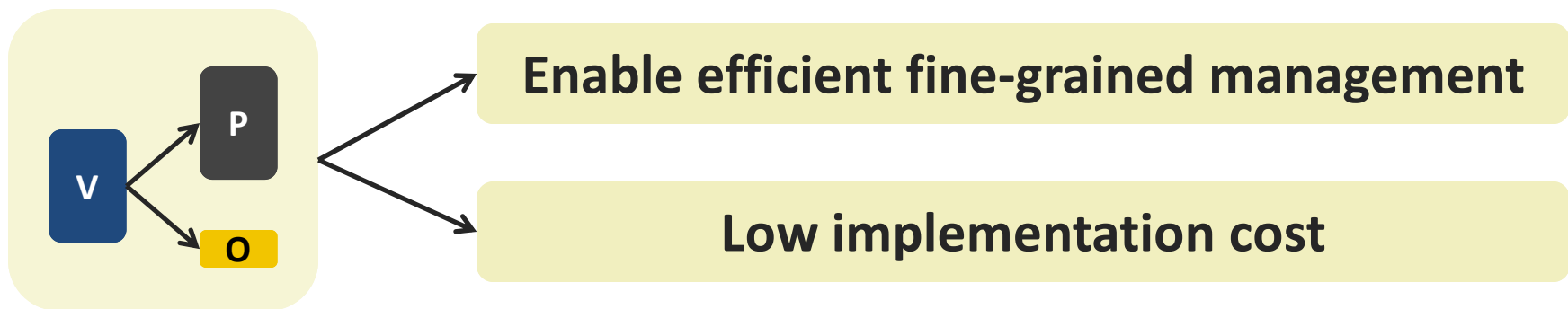


Goal: Efficient Fine-grained Memory Management

Existing Virtual Memory Framework



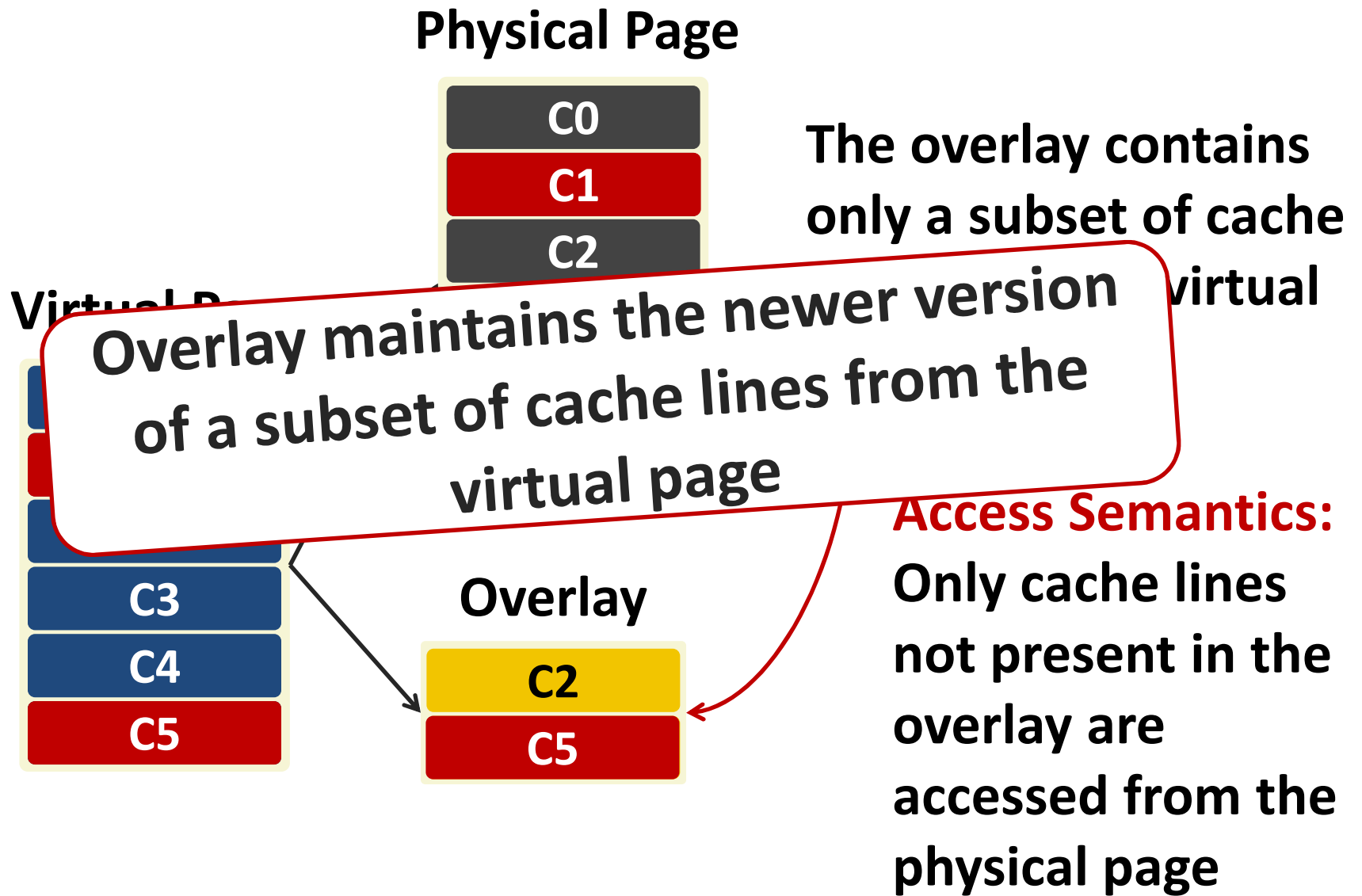
New Virtual Memory Framework



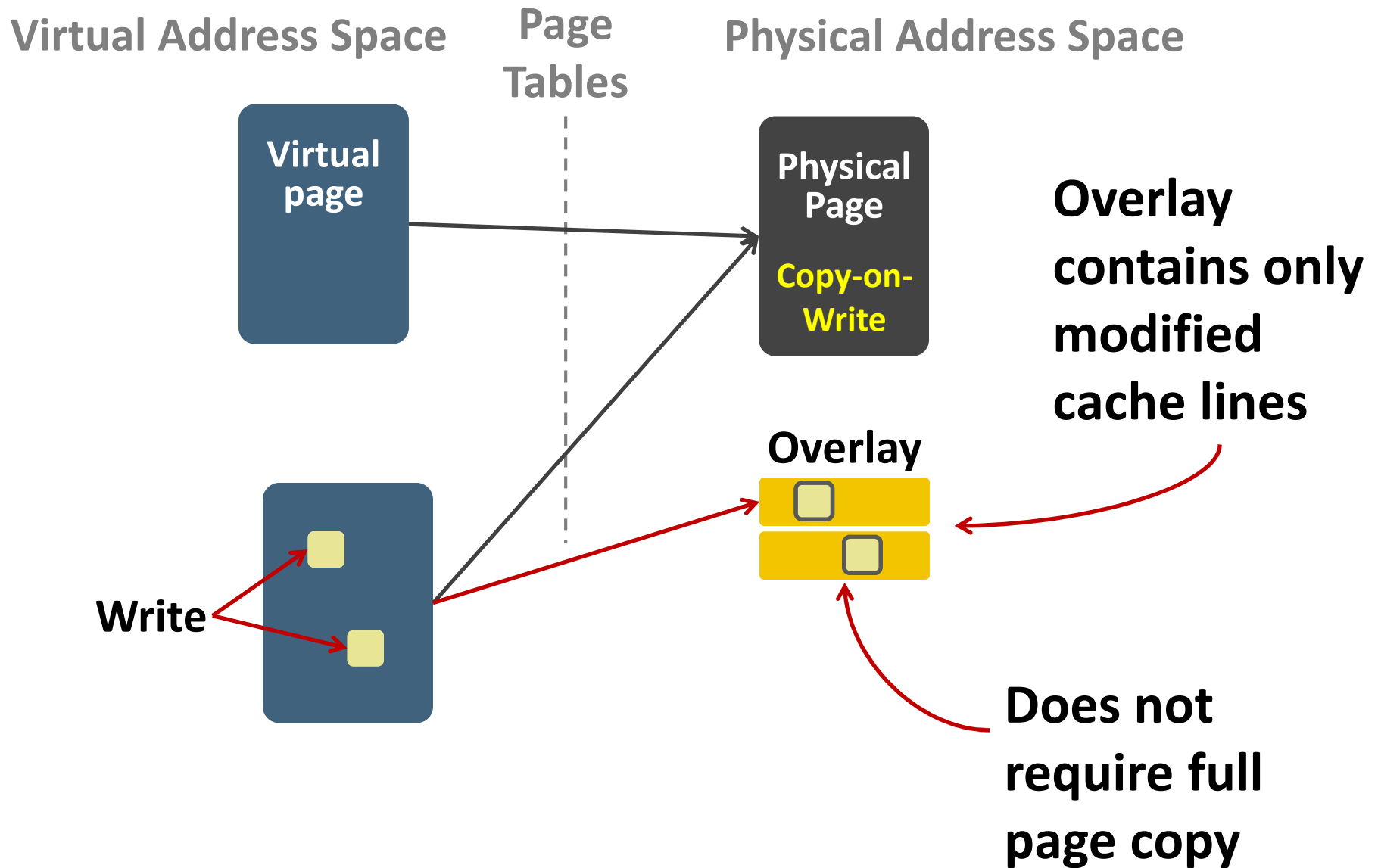
Outline

- Shortcomings of Existing Framework
- Page Overlays – Overview
- Implementation
 - Challenges and solutions
- Applications and Evaluation
- Conclusion

The Page Overlay Framework



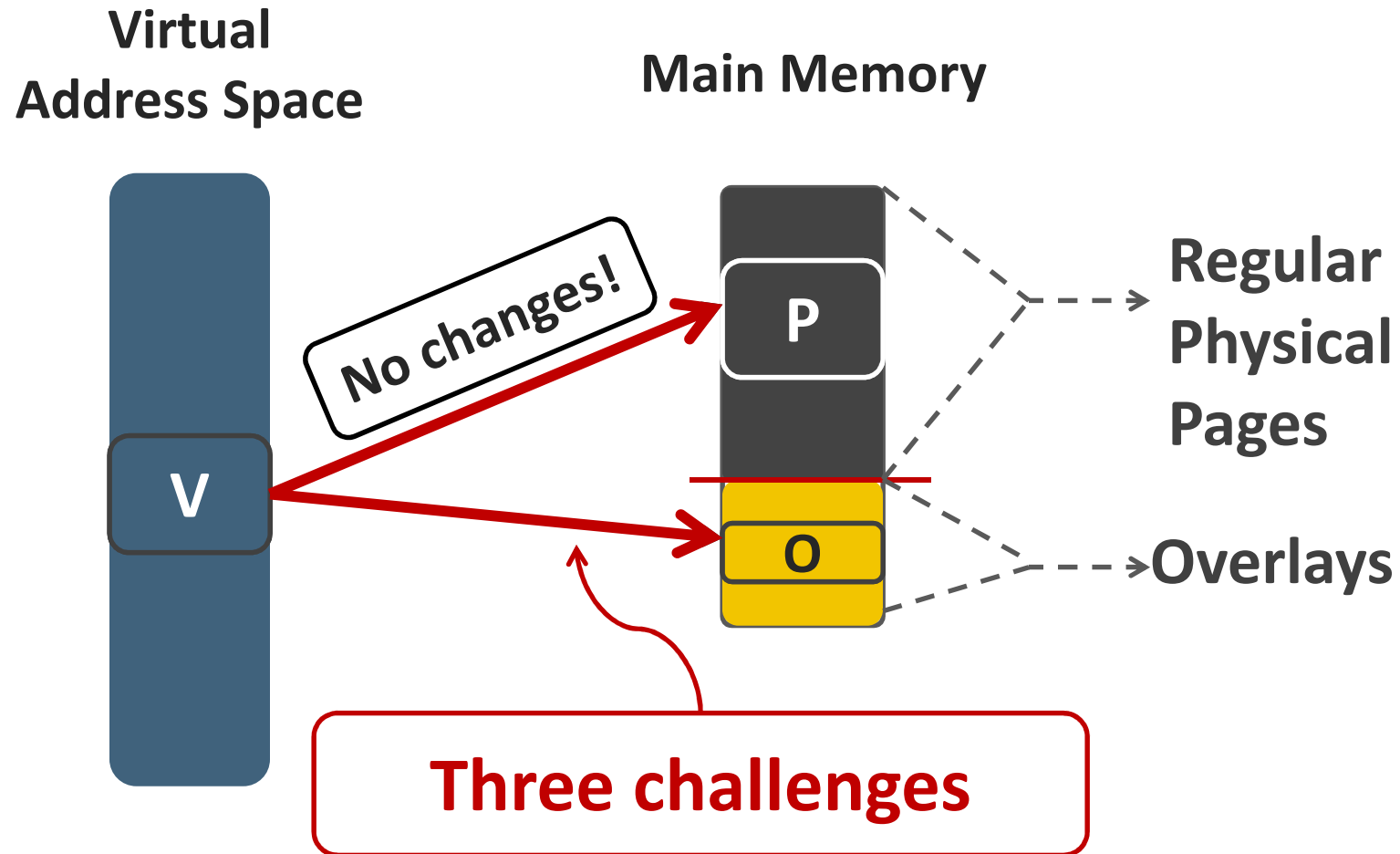
Overlay-on-Write: An Efficient Copy-on-Write



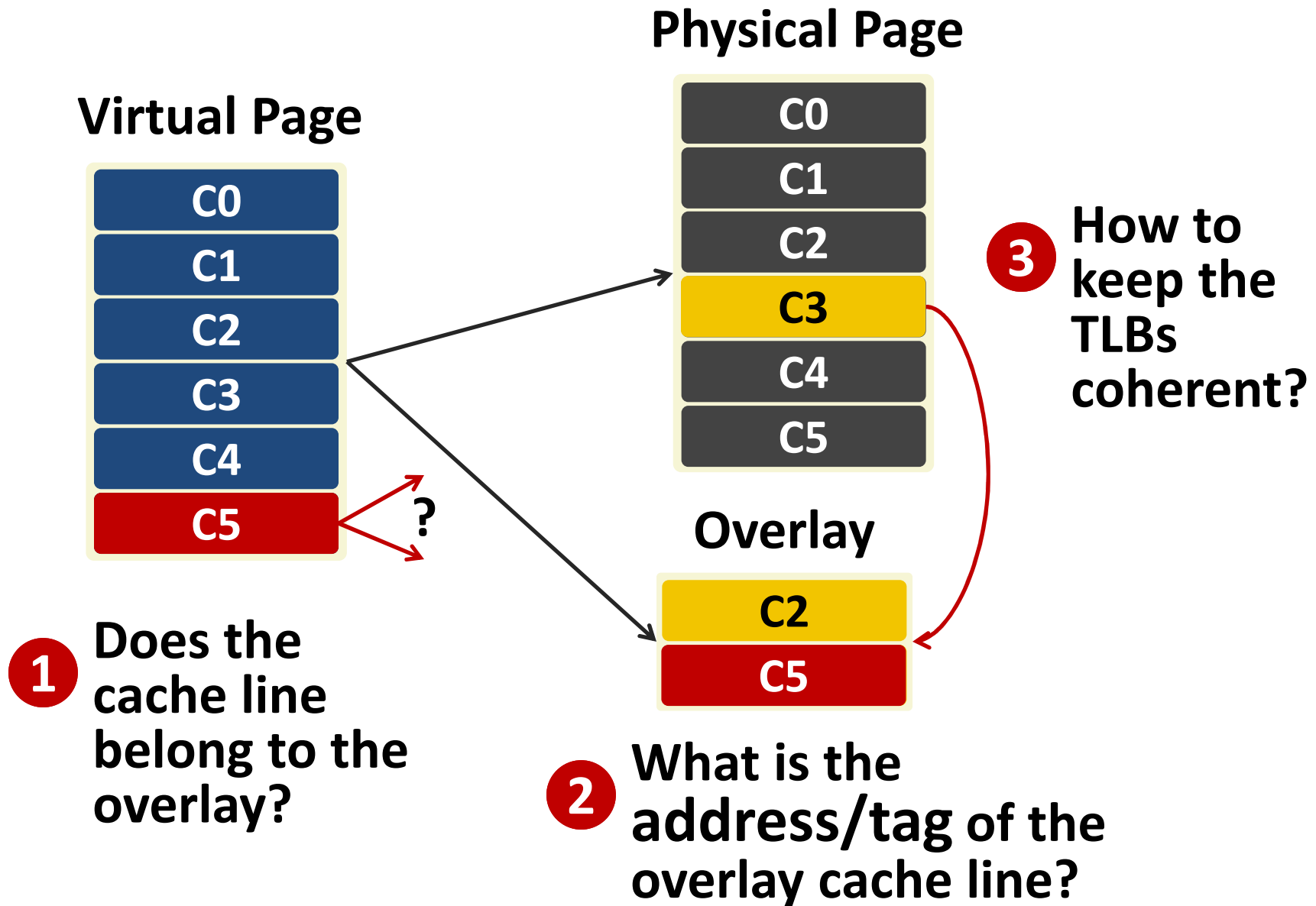
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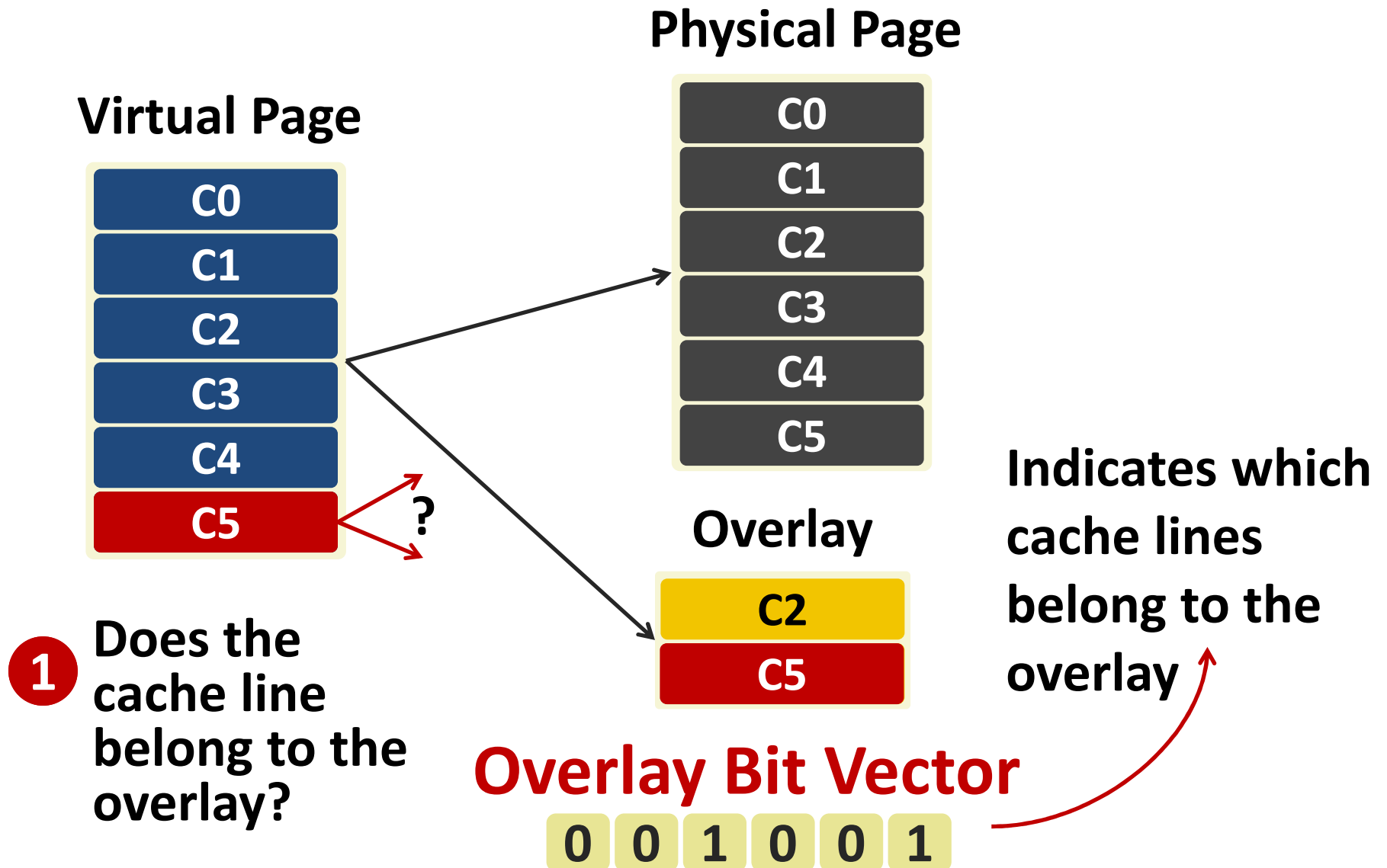
Implementation Overview



Implementation Challenges



Identifying Overlay Cache Lines: Overlay Bit Vector



Addressing Overlay Cache Lines: Naïve Approach

Virtual
Address Space



Main Memory



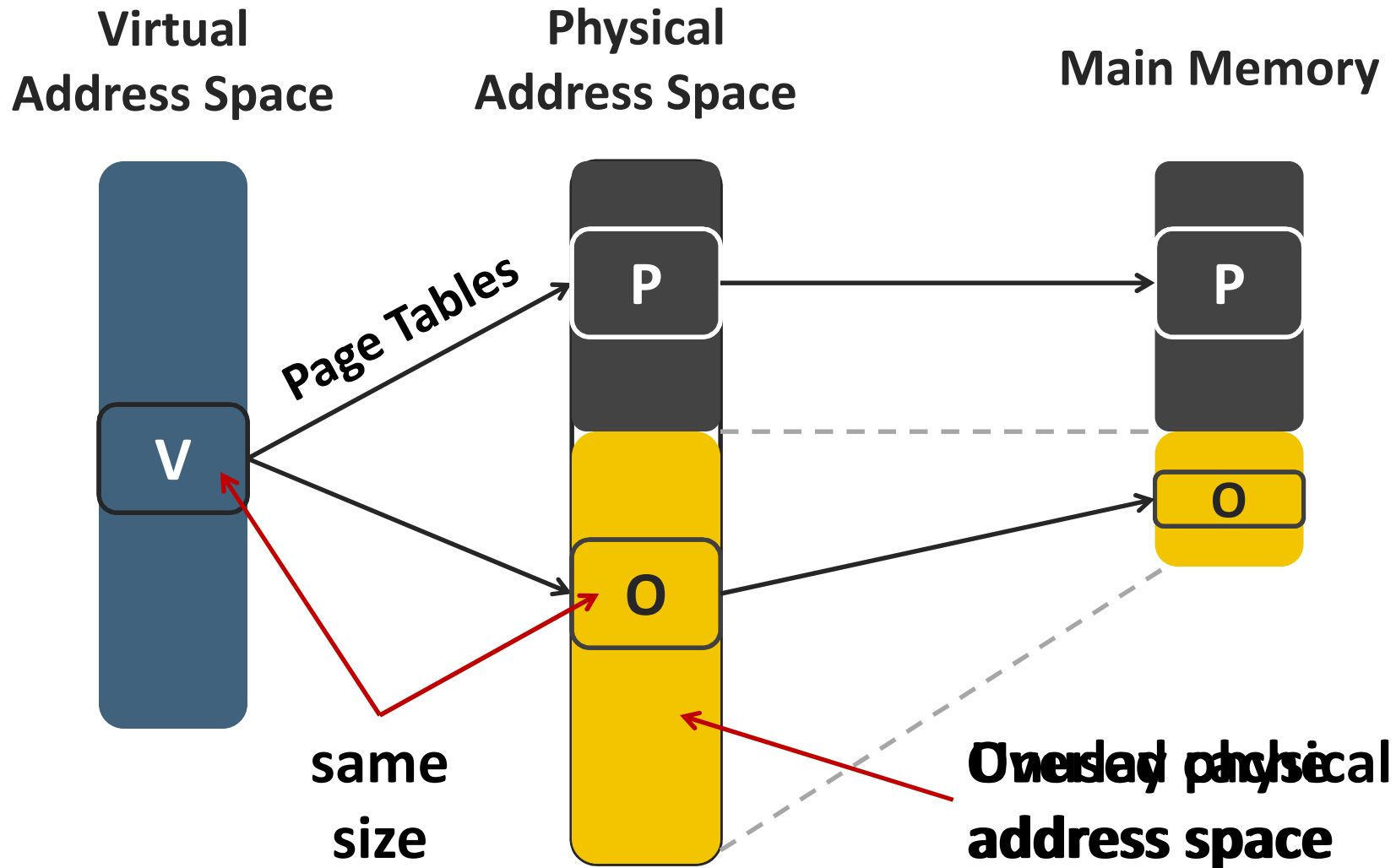
Use the location of
the overlay in main
memory to tag
overlay cache lines

1. Processor must compute the address

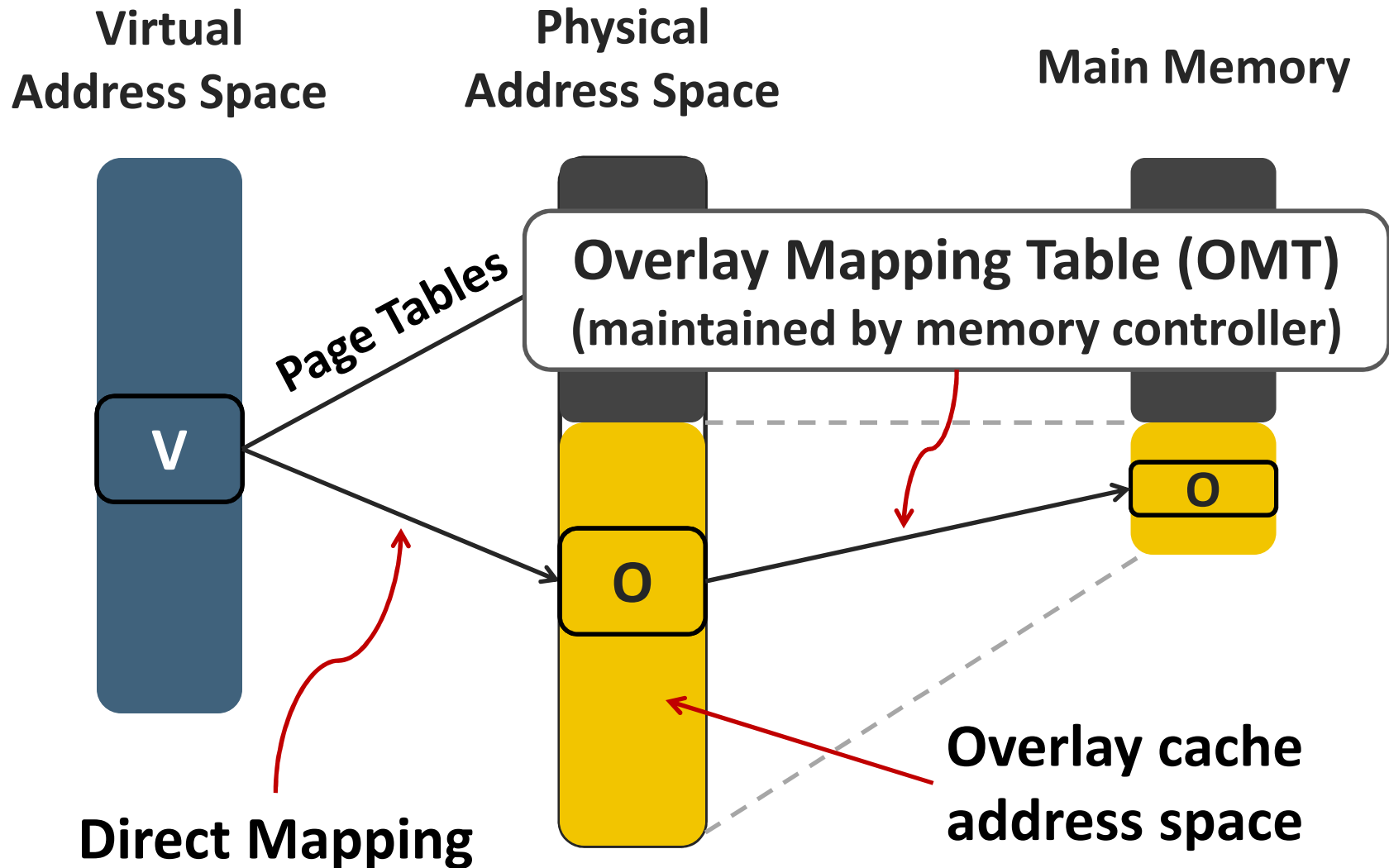
2. Does not work with virtually-indexed caches

3. Complicates overlay cache line insertion

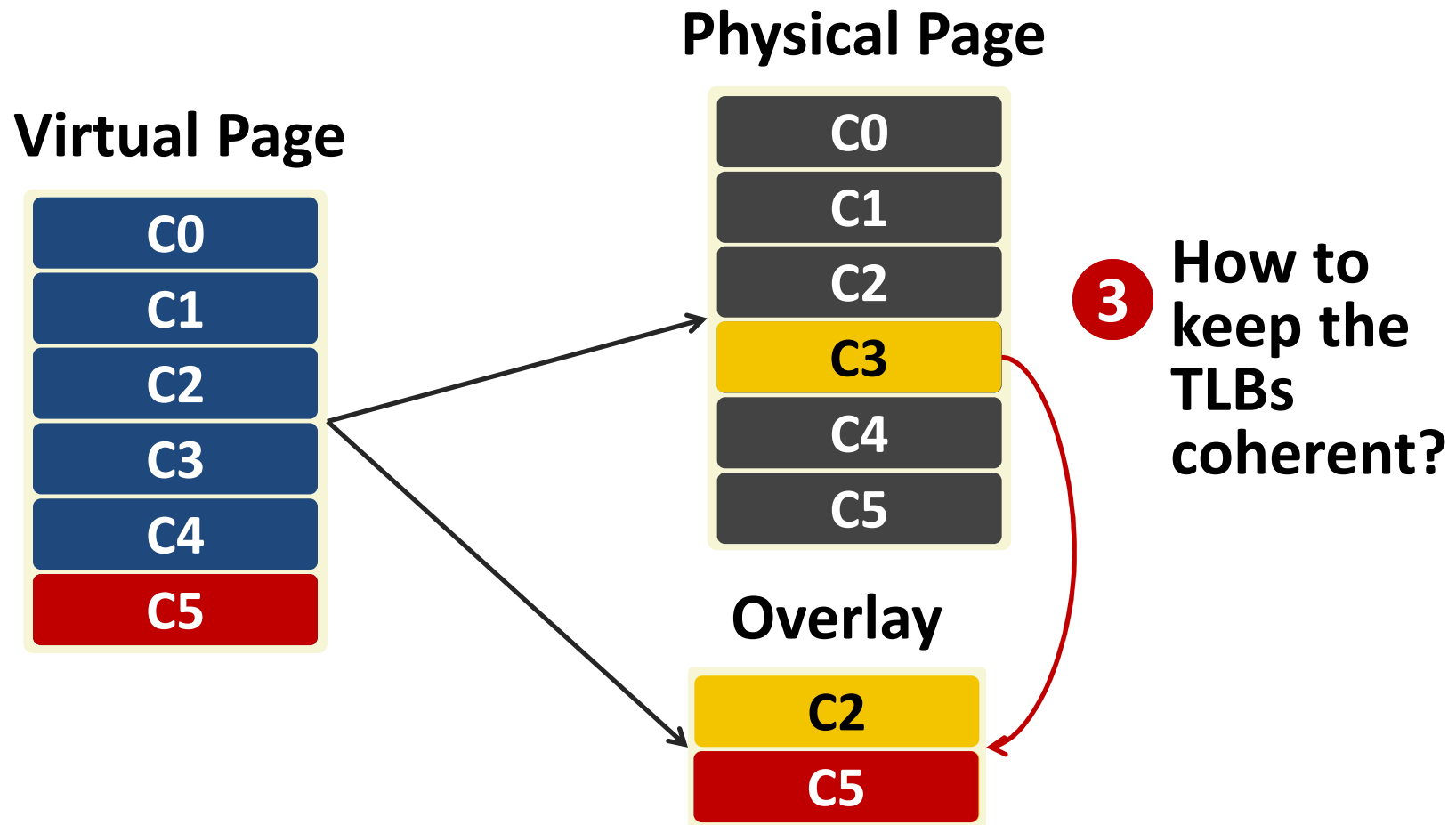
Addressing Overlay Cache Lines: Dual Address Design



Virtual-to-Overlay Mappings

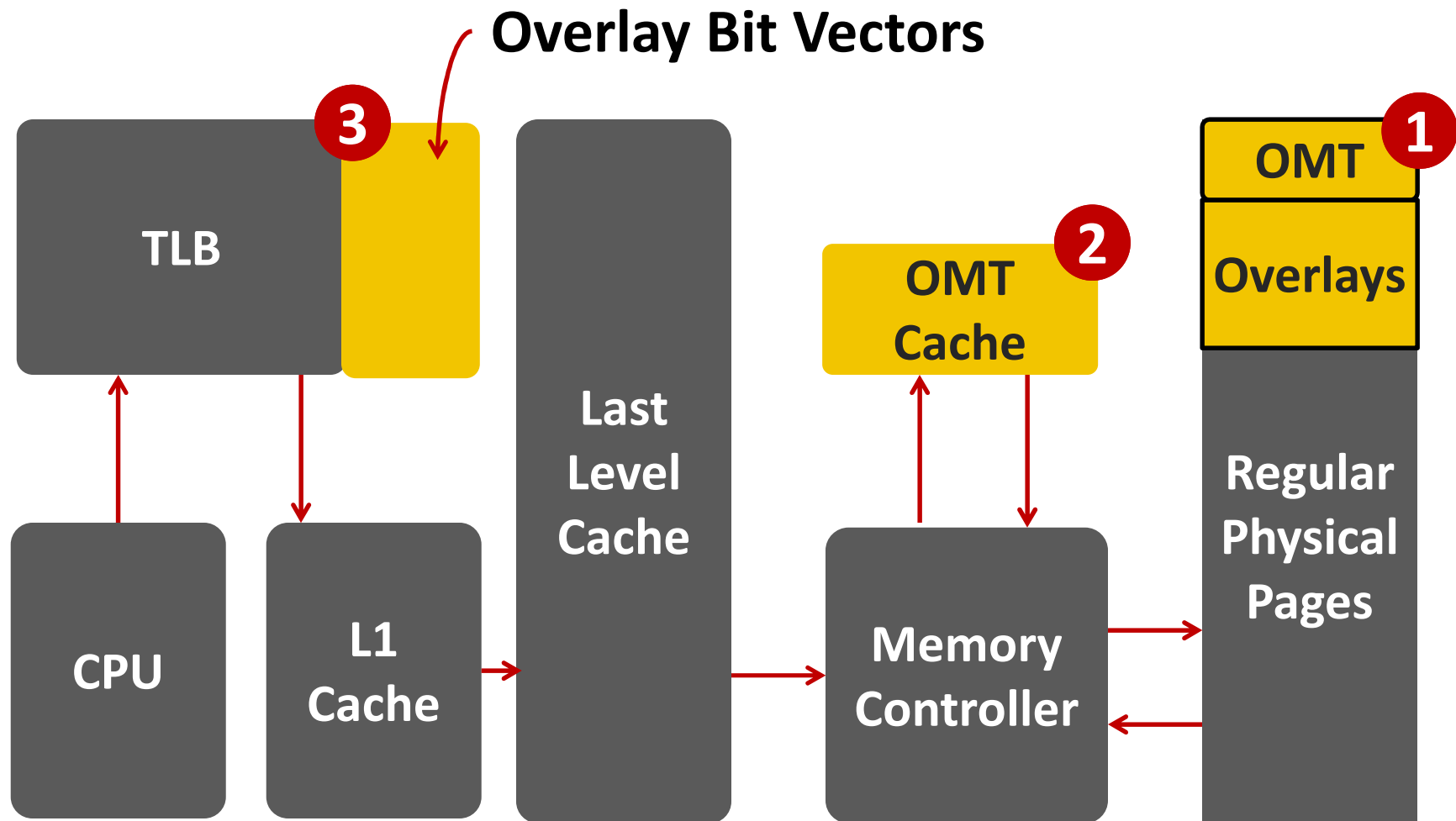


Keeping TLBs Coherent



Use the cache coherence protocol to keep TLBs coherent!

Final Implementation



Other Details in the Paper

- **Virtual-to-overlay mapping**
- **TLB and cache coherence**
- **OMT management (by the memory controller)**
- **Hardware cost**
 - 94.5 KB of storage
- **OS Support**

Outline

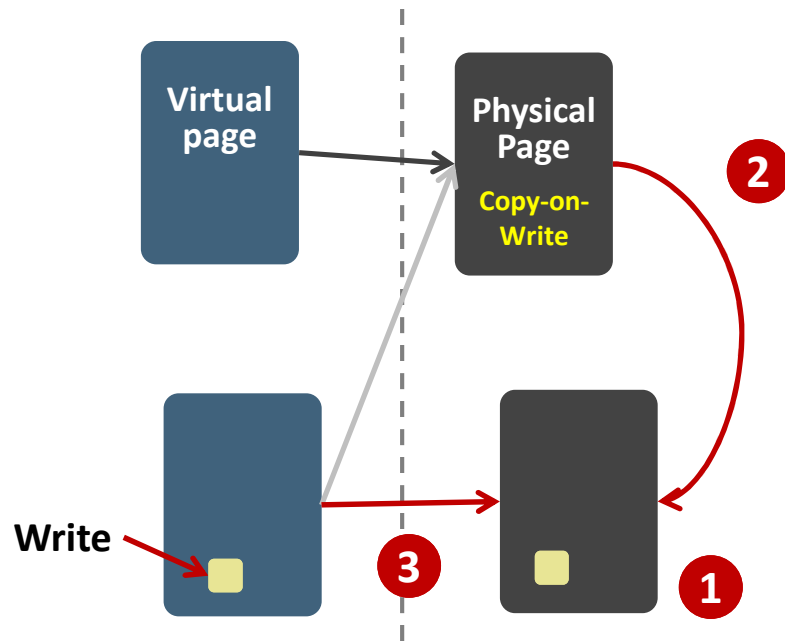
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Methodology

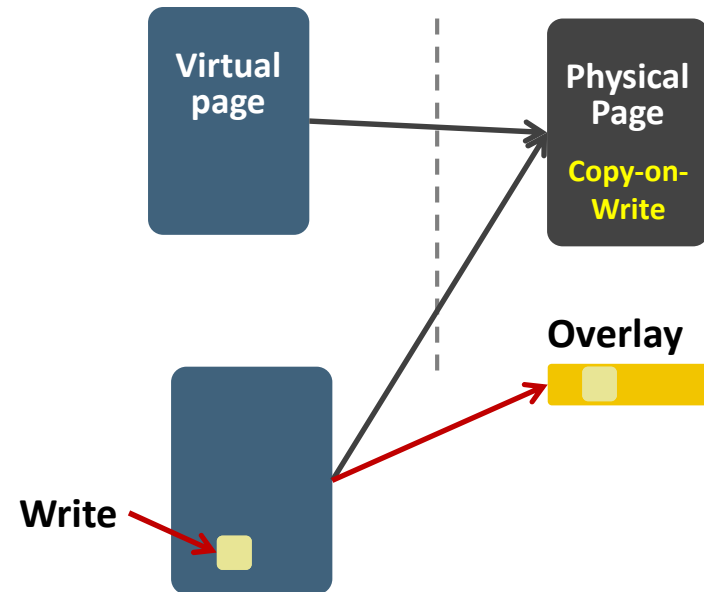
- Memsim memory system simulator [Seshadri+ PACT 2012]
- 2.67 GHz, single core, out-of-order, 64 entry instruction window
- **64-entry L1 TLB, 1024-entry L2 TLB**
- **64KB L1 cache, 512KB L2 cache, 2MB L3 cache**
- Multi-entry Stream Prefetcher [Srinath+ HPCA 2007]
- Open row, FR-FCFS, 64 entry write buffer, drain when full
- **64-entry OMT cache**
- DDR3 1066 MHz, 1 channel, 1 rank, 8 banks

Overlay-on-Write

Copy-on-Write

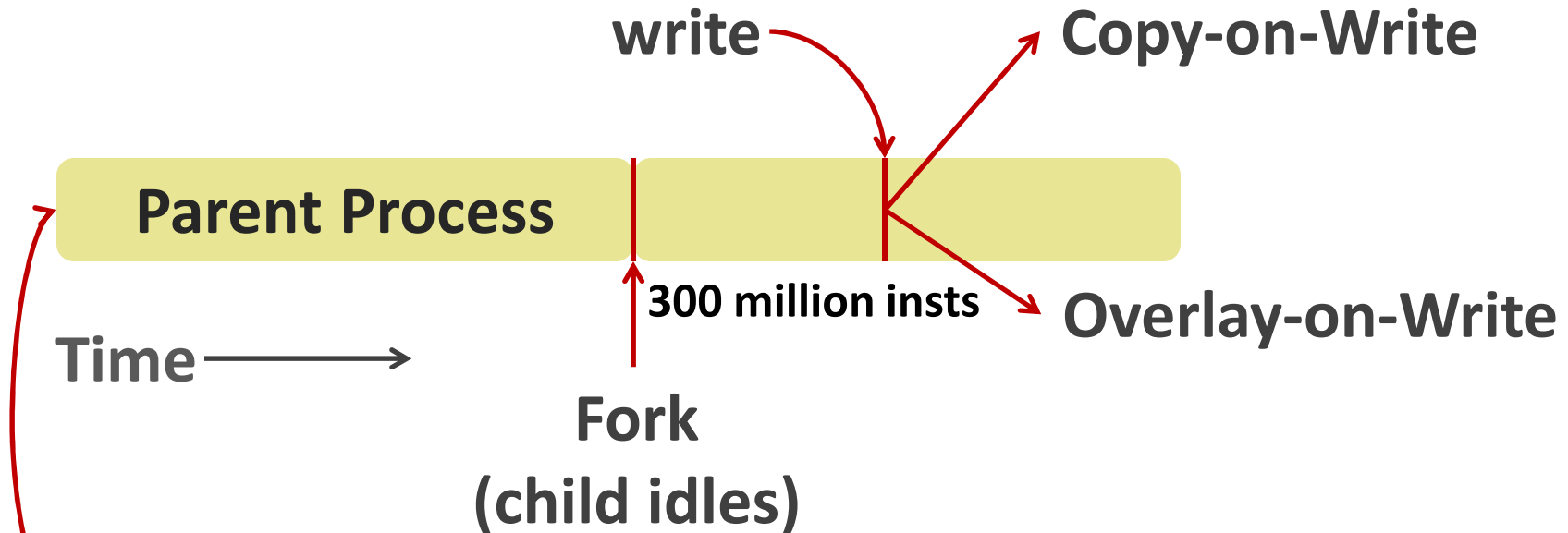


Overlay-on-Write



- Lower memory redundancy
- Lower latency

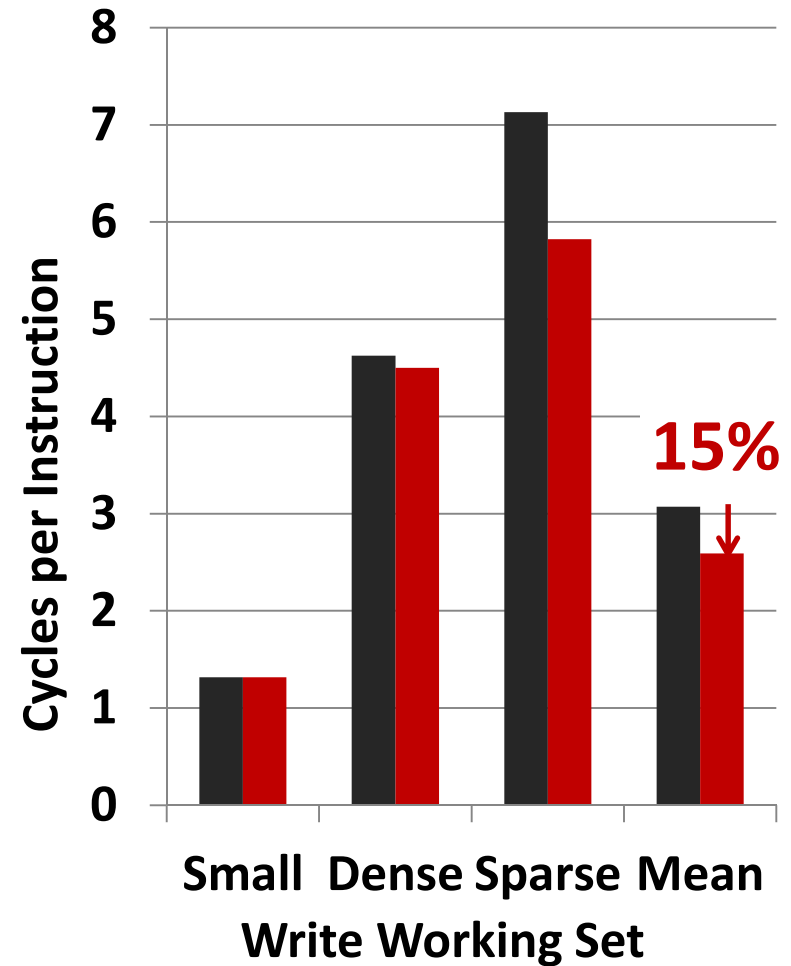
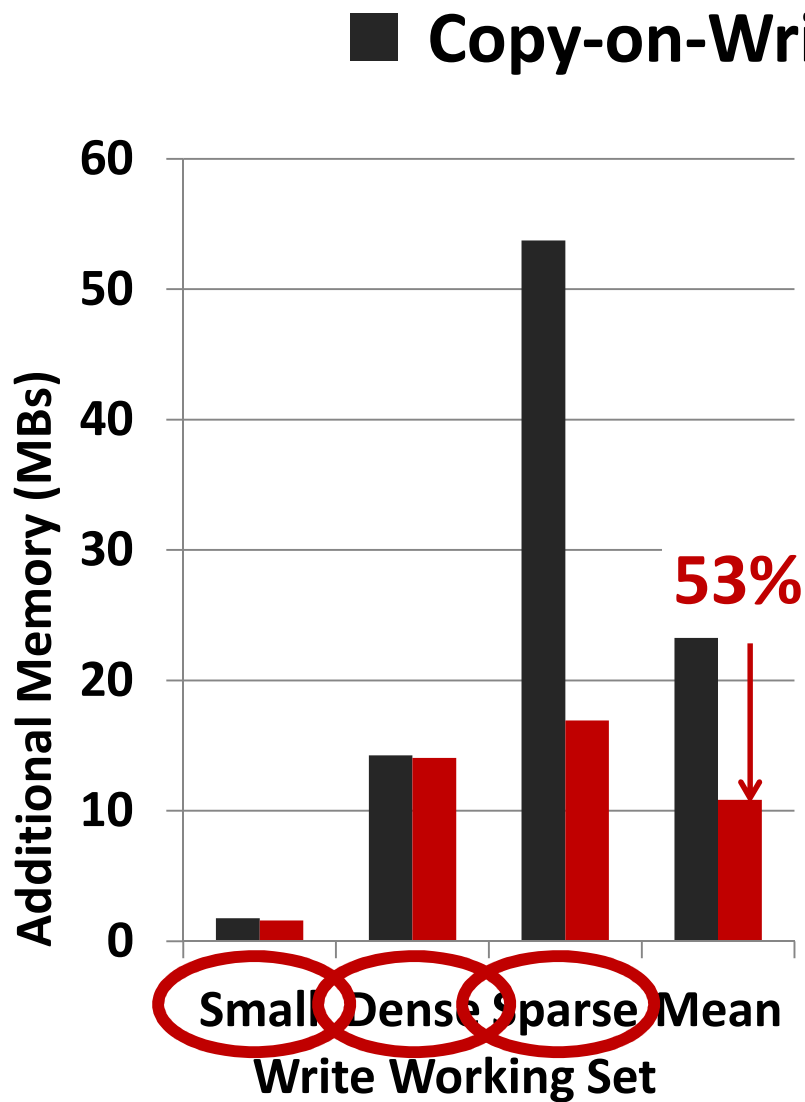
Fork Benchmark



Applications from SPEC CPU 2006 (varying write working sets)

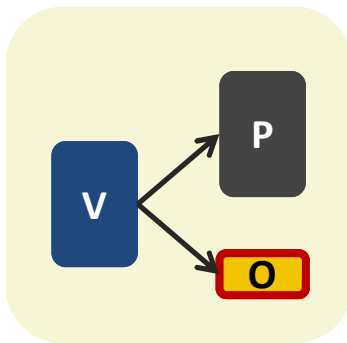
- Additional memory consumption
- Performance (cycles per instruction)

Overlay-on-Write vs. Copy-on-Write on Fork



Conclusion

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