Flipping Bits in Memory Without Accessing Them:

DRAM Disturbance Errors

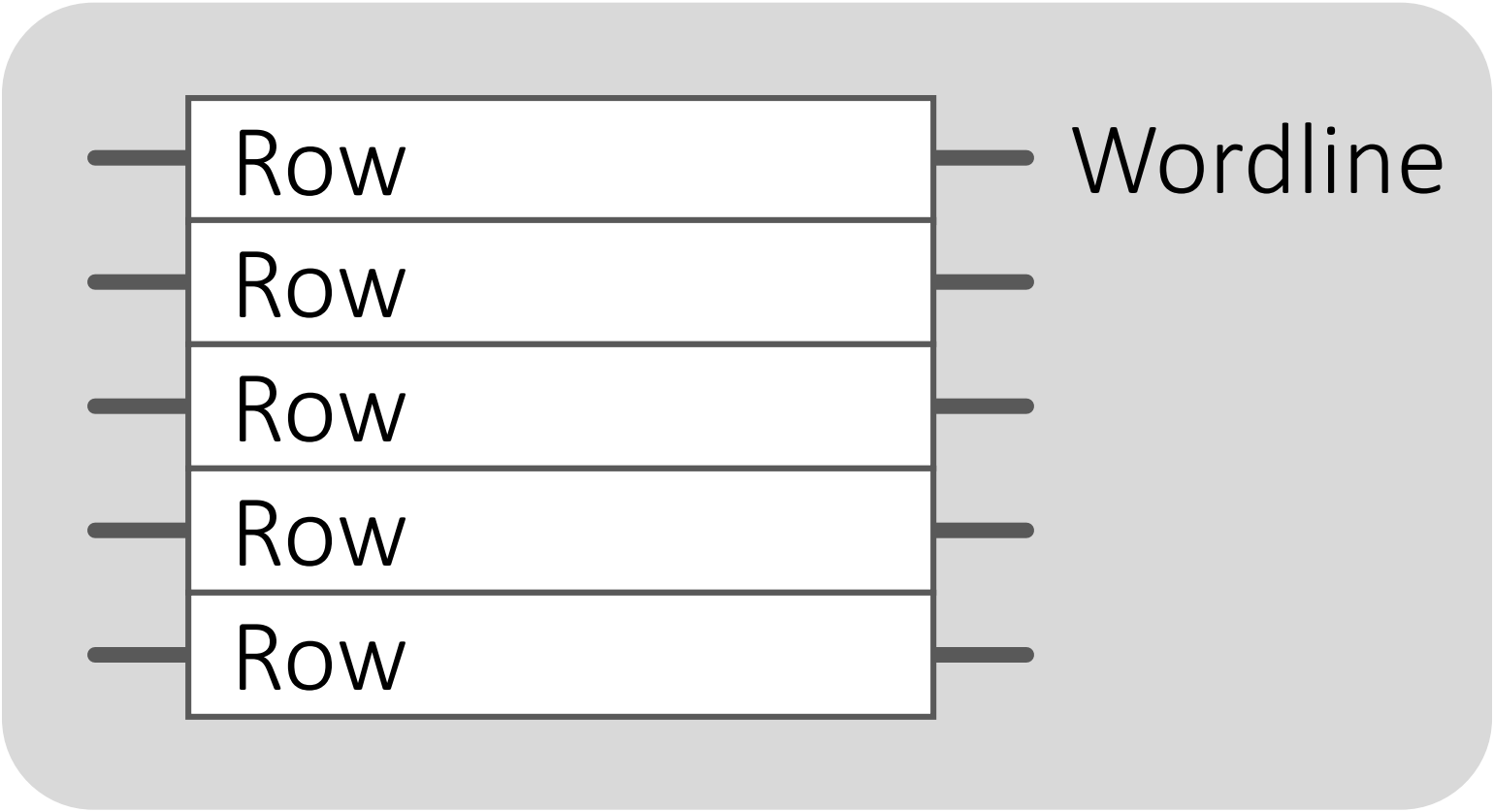
Yoongu Kim

Ross Daly, Jeremie Kim, Chris Fallin, Ji Hye Lee,

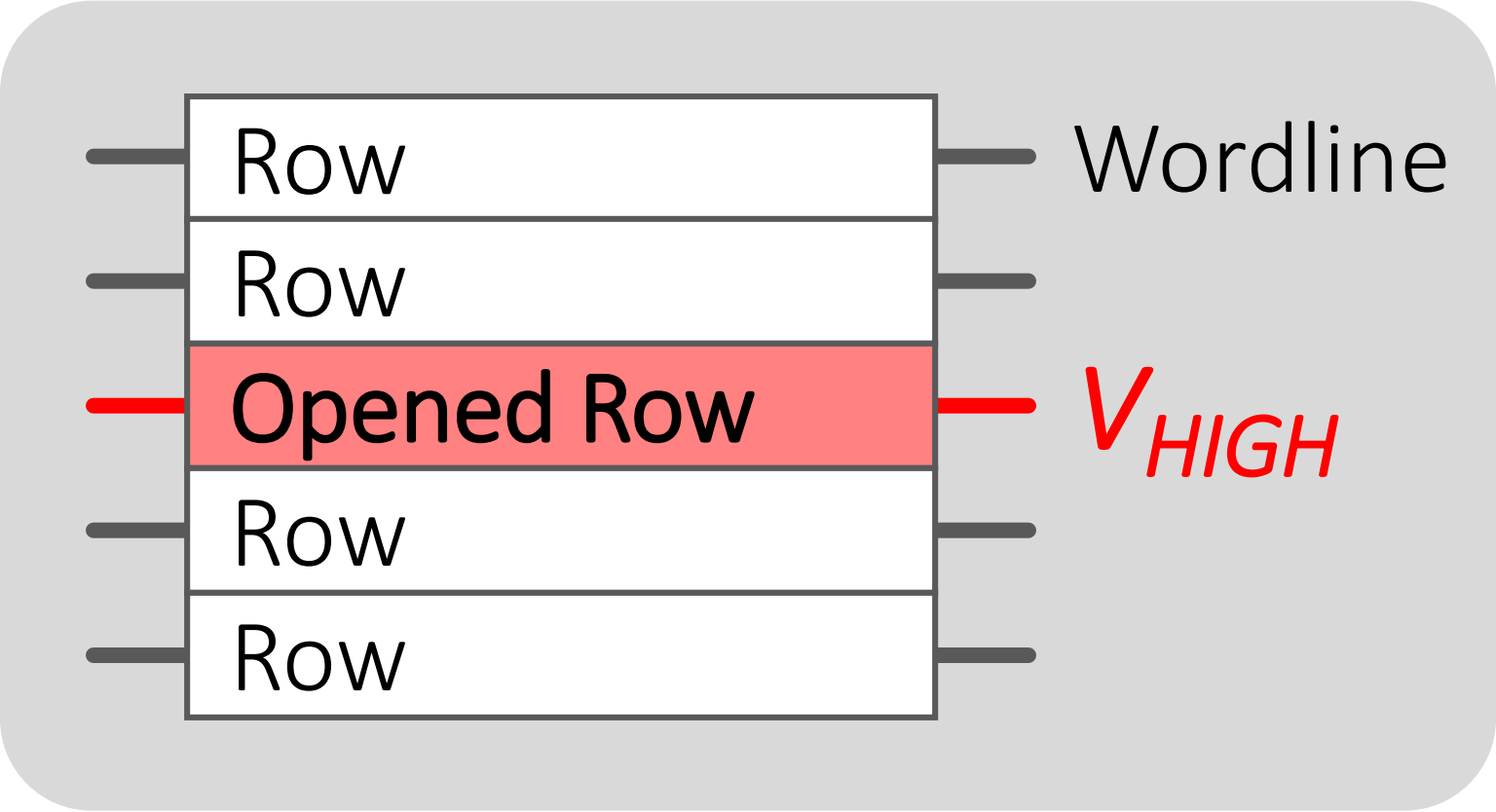
Donghyuk Lee, Chris Wilkerson, Konrad Lai, Onur Mutlu

Carnegie Mellon SAFARI intel

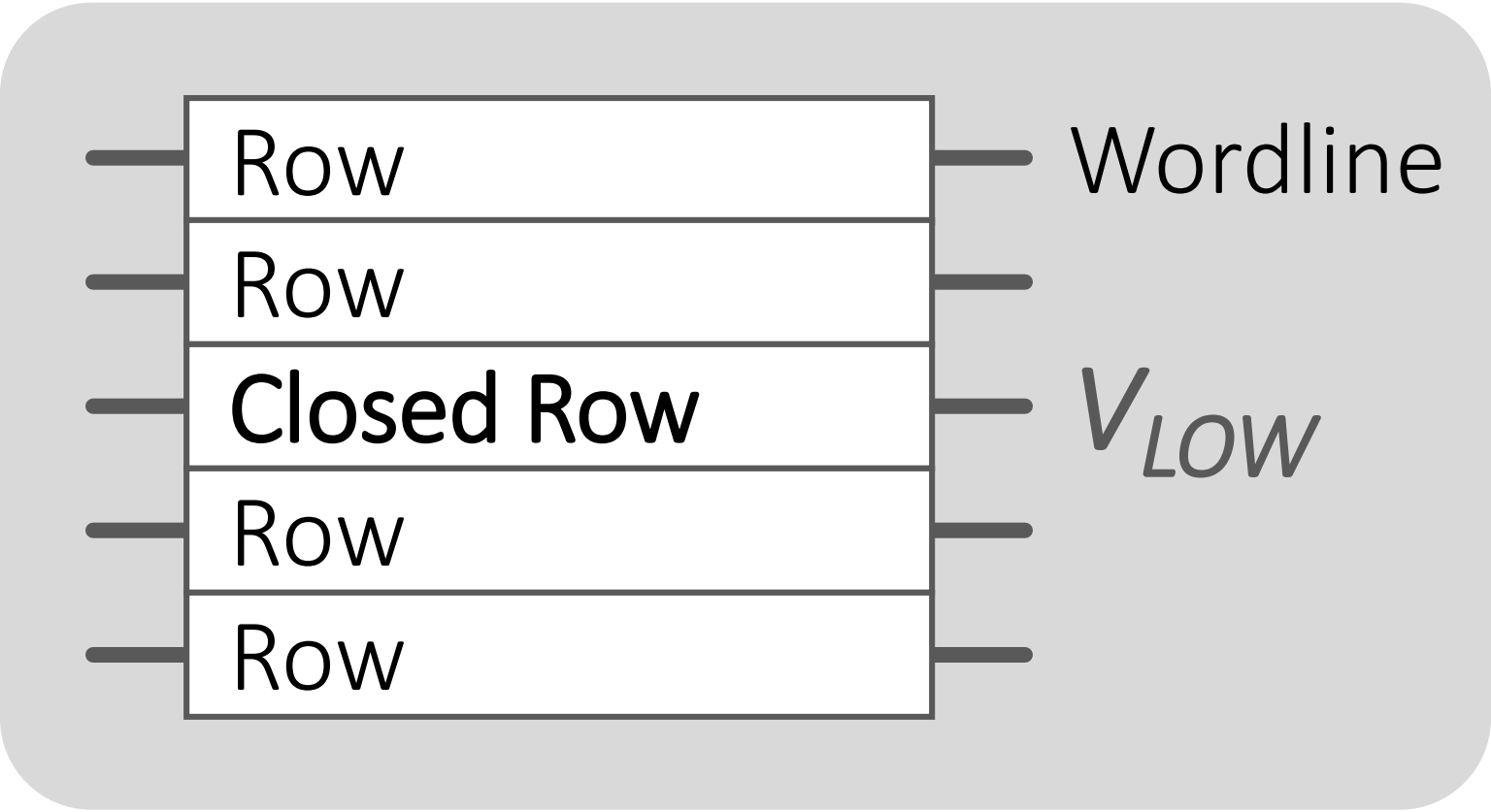
DRAM Chip



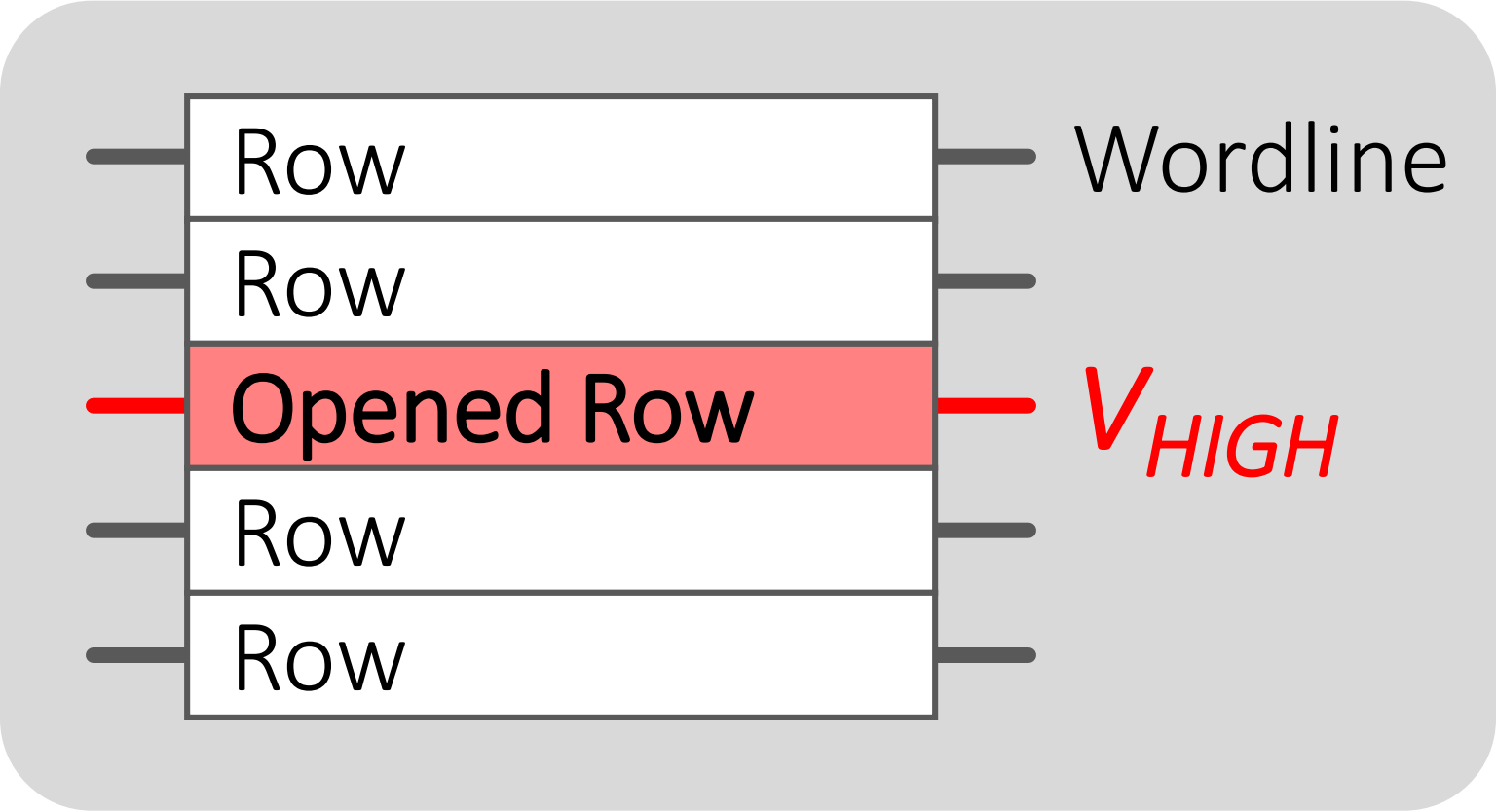
DRAM Chip



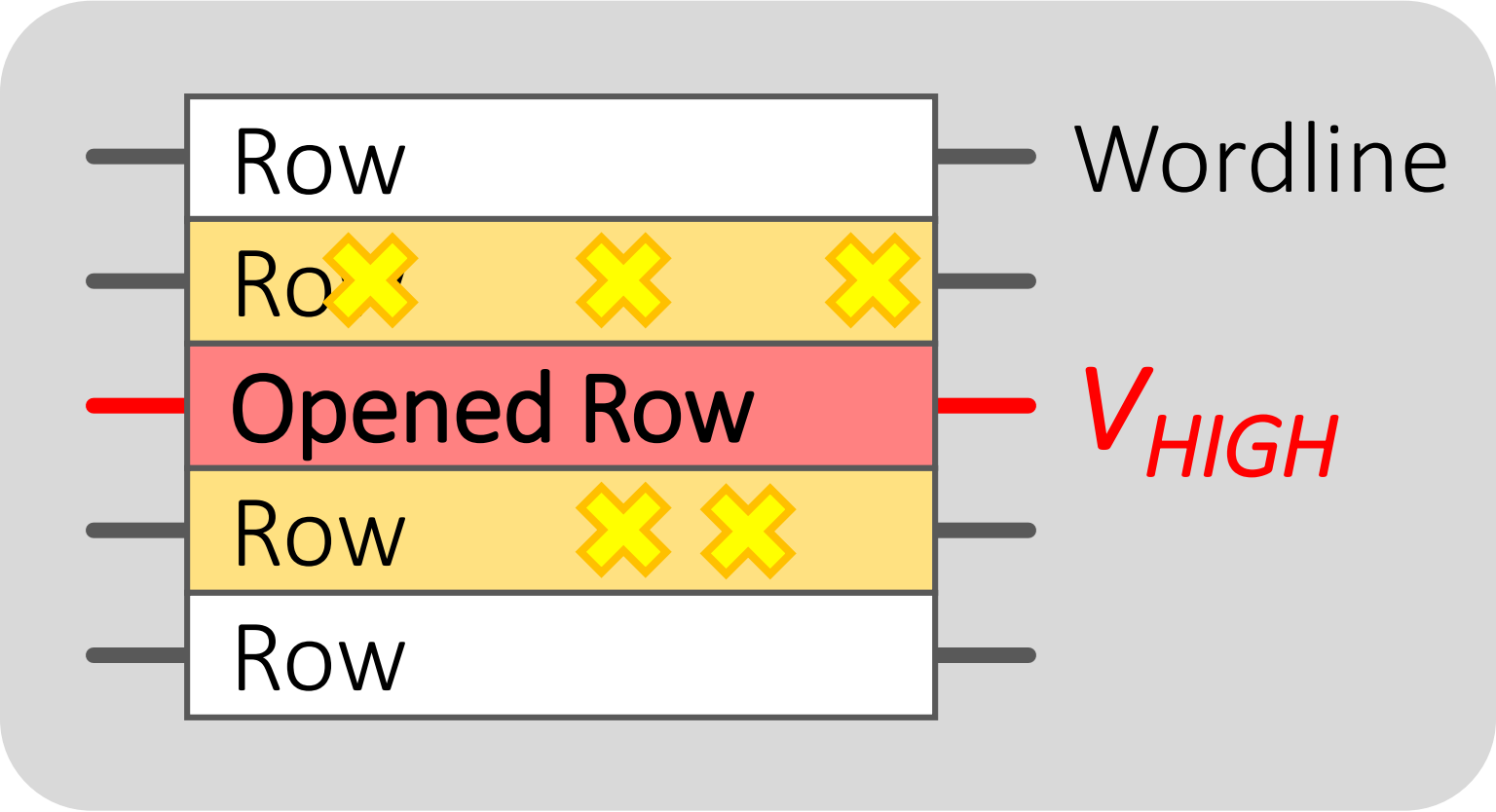
DRAM Chip



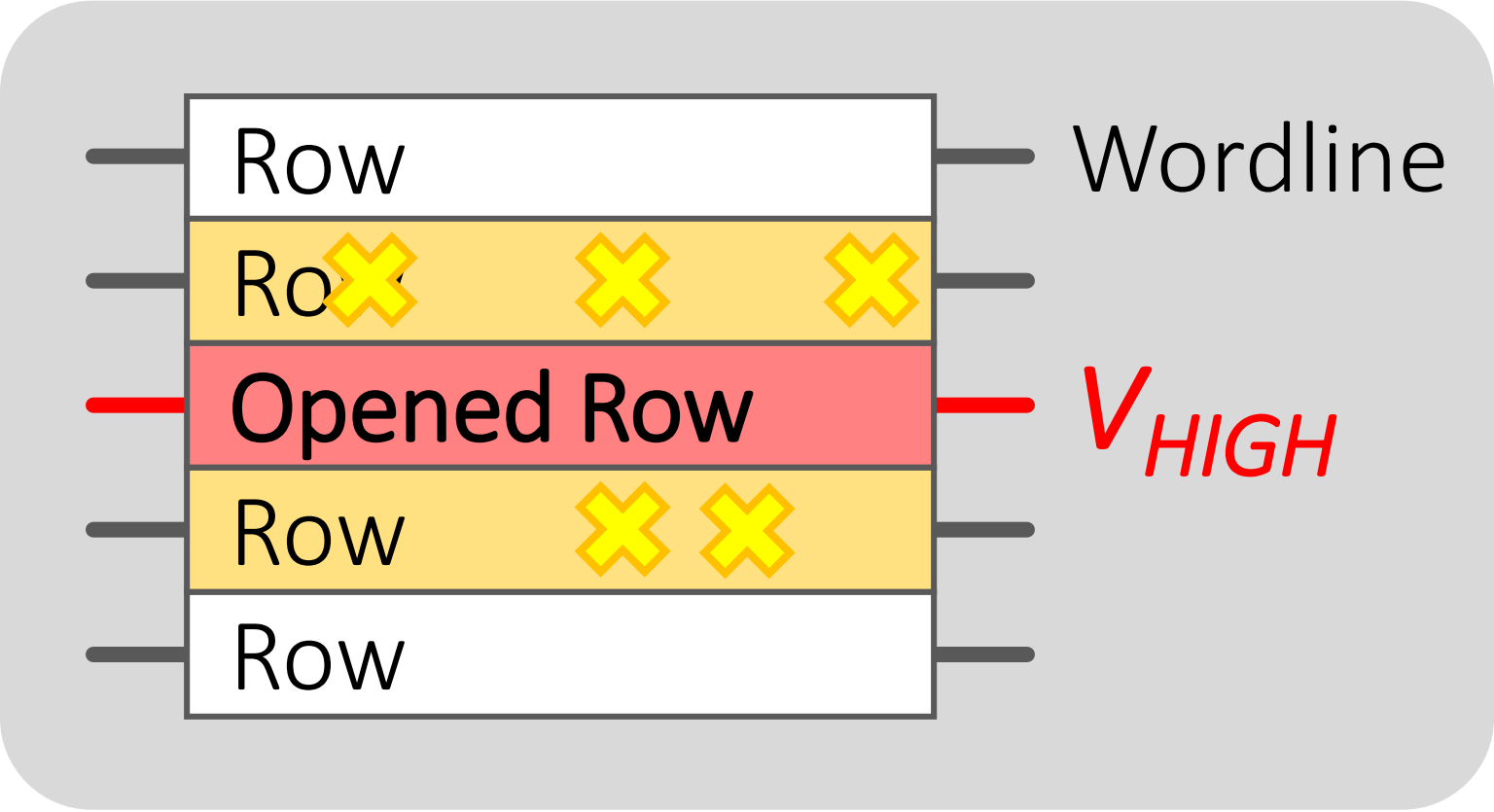
DRAM Chip



DRAM Chip



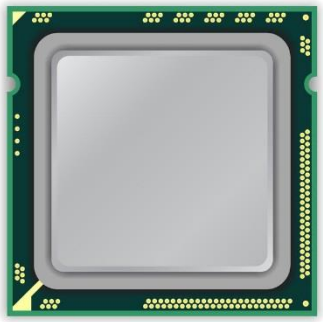
DRAM Chip

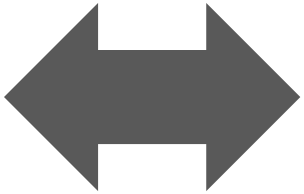


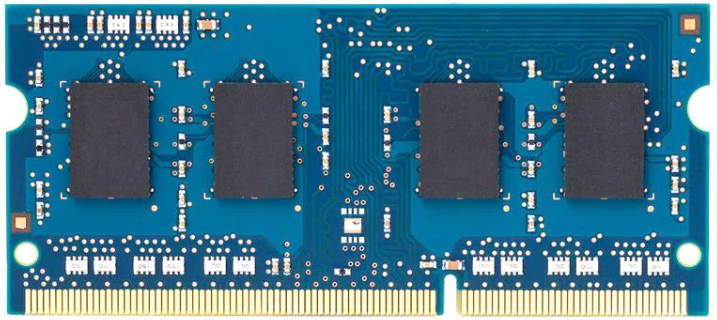
Repeatedly opening and closing a row induces ***disturbance errors*** *in adjacent rows*

x86 CPU

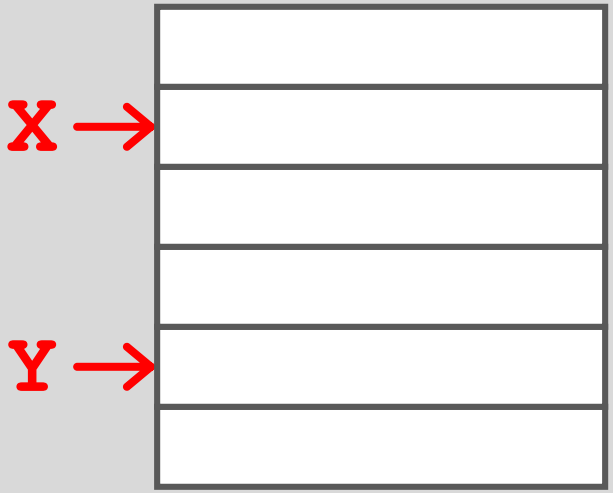
DRAM Module



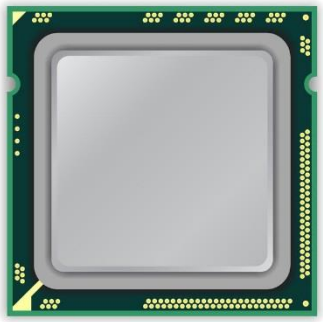




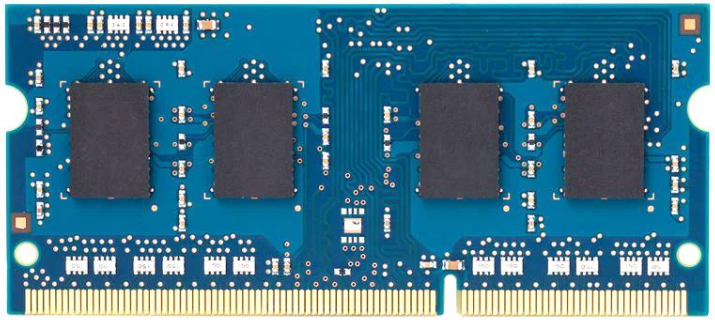
```
loop:
   mov (X), %eax
   mov (Y), %ebx
   clflush (X)
   clflush (Y)
   mfence
   jmp loop
```



x86 CPU



DRAM Module



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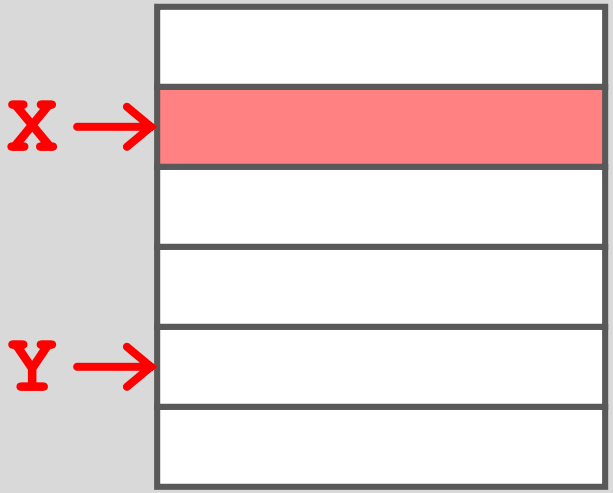
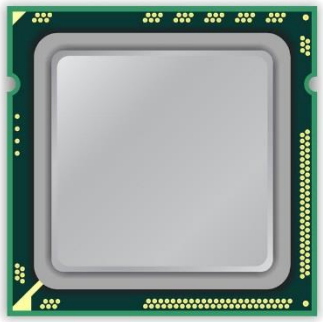
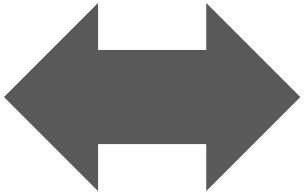
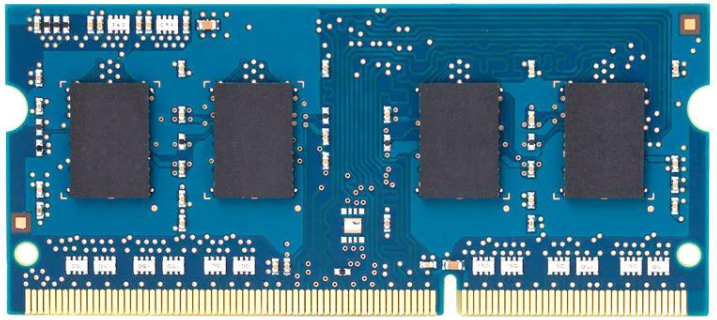


x86 CPU

DRAM Module







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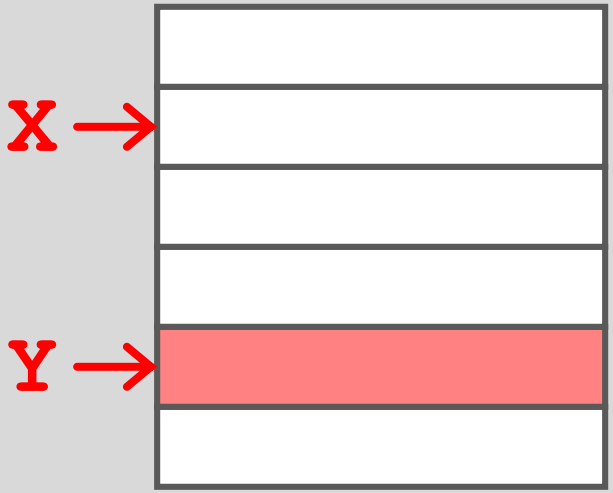
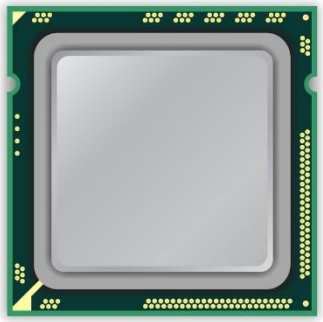
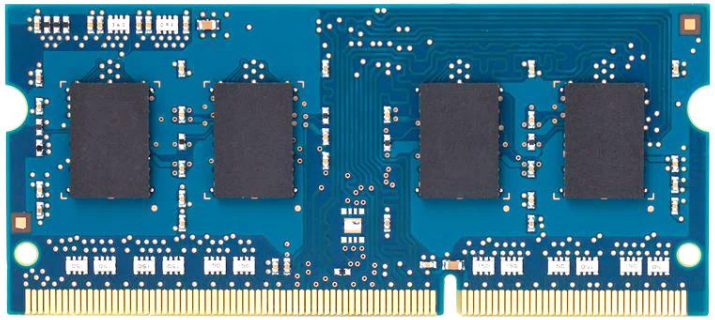


x86 CPU



DRAM Module



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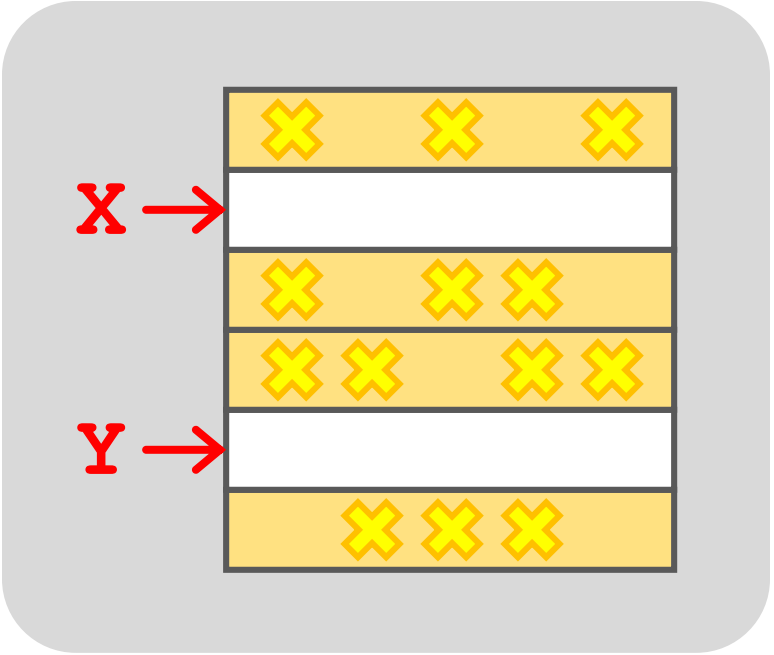
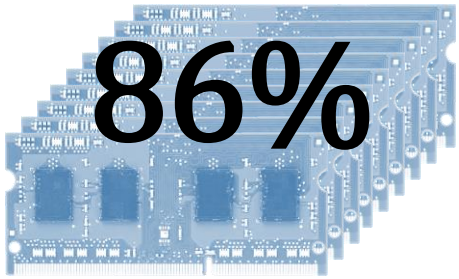
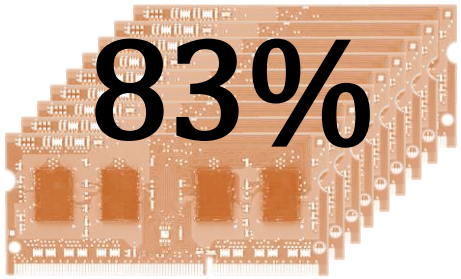
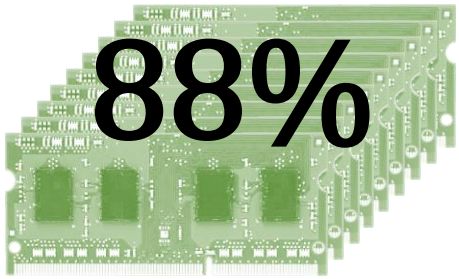


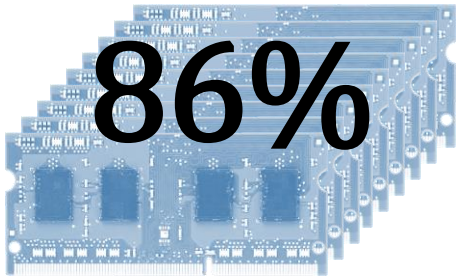
Most Modules At Risk



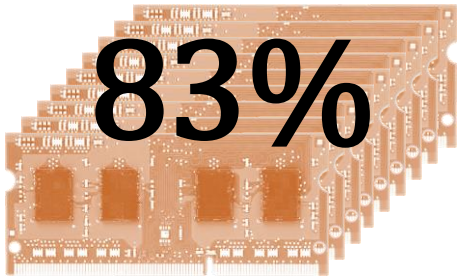




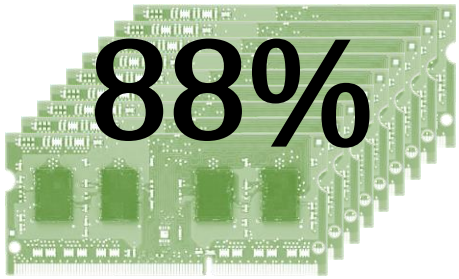
Most Modules At Risk



After
2010

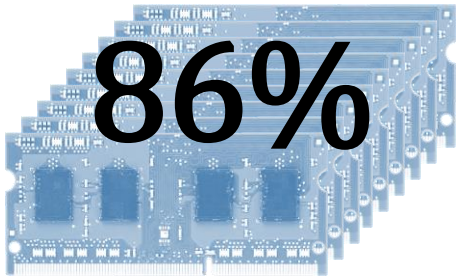


After
2010



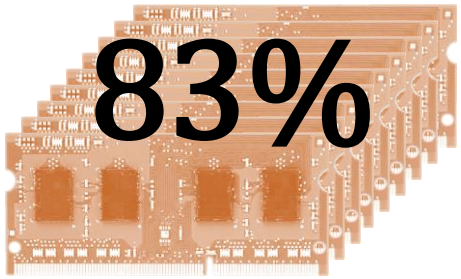
After
2009

Most Modules At Risk



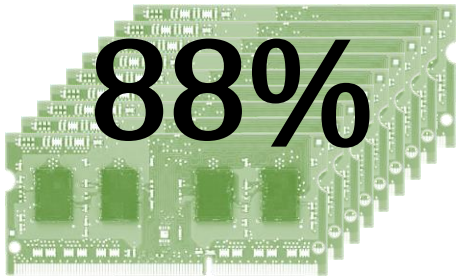
After
2010

10^7
Errors



After
2010

10^6
Errors



After
2009

10^5
Errors

Flipping Bits in Memory Without Accessing Them:

DRAM Disturbance Errors

4:30 PM

Carnegie Mellon SAFARI intel