# SIA Road Map
# and
# DESIGN&TEST

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**Pittsburgh, Pa. 15213.**

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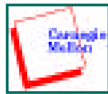
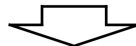
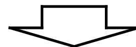


# Objective

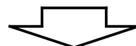
**To discuss fundamental research in**
**Design and Test (D&T) of VLSI ICs**



**D&T Current and Future Problems**



**Future of IC Technology**



**SIA Road Map**

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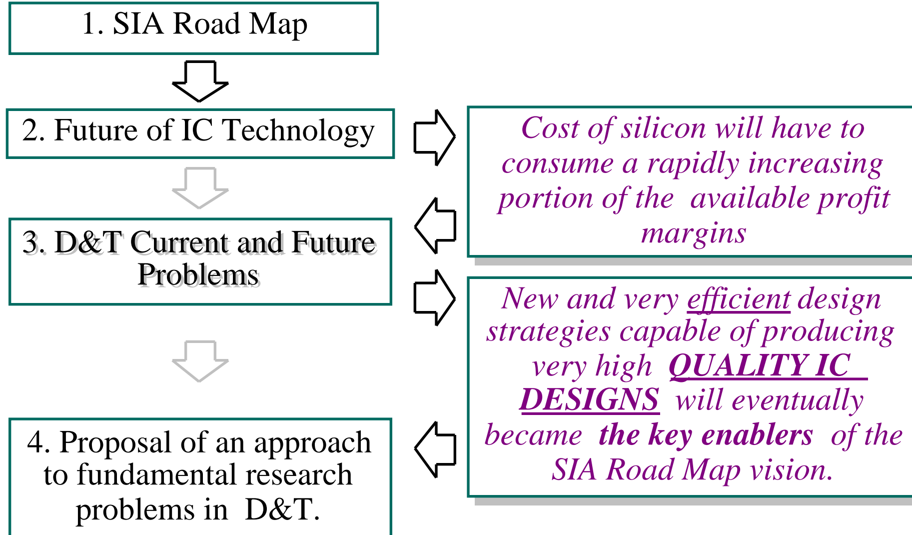
# Outline

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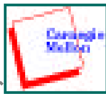
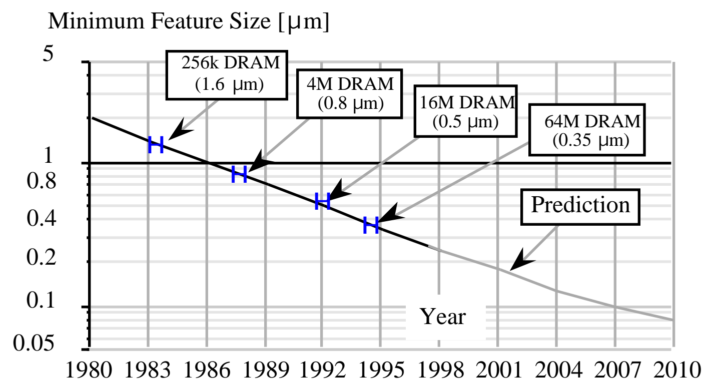


# SIA Road Map

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# 1994 SIA Road Map Assumptions

| Year | 1995 | 1998 | 2001 | 2004 | 2007 | 2010 |
|---|---|---|---|---|---|---|
| Feature size [µm] | **0.35** | **0.25** | **0.18** | **0.12** | **0.1** | **0.08** |
| Wafer diameter [mm] | **200** | **200** | **300** | **300** | **400** | **400** |
| | | | **M E M O R Y** | | | |
| Tr. per chip [10 6] | **64** | **256** | **1024** | **4096** | **16384** | **65536** |
| Cost per tr. [millicents] | **0.017** | **0.007** | **0.003** | **0.001** | **0.0005** | **0.0002** |
| Chip size [mm $^2$] | **190** | **280** | **420** | **640** | **960** | **1400** |
| Tr. density [10 $^6$ # tr. / cm $^2$ ] | **34** | **91** | **244** | **640** | **1707** | **4681** |
| | | | **µ P R O C S S O R** | | | |
| Tr. per chip [10 $^6$] | **10** | **21** | **46.8** | **107.5** | **260** | **558** |
| Cost per tr. [millicents] | **1** | **0.5** | **0.2** | **0.1** | **0.05** | **0.02** |
| Chip size [mm $^2$] | **250** | **300** | **360** | **430** | **520** | **620** |
| Tr. density [10 $^6$ # tr. / cm $^2$ ] | **4** | **7** | **13** | **25** | **50** | **90** |

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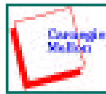

# SIA Road Map

- SIA Road Map is a collective view on the future of the microelectronics industry;
- The objective of the SIA Road Map was a consolidation of the vision for the entire semiconductor industry;
- Such a consolidation was a necessary step in focusing industry, governments and universities on the same technology development objectives;
- The SIA Road Map has a strong “technology/ manufacturing/ equipment” orientation;
- The SIA Road Map is a “linear extrapolation” of the trends known from the past;
- The SIA Road Map is a “self-fulfilling prophecy” which facilitates continuation of the evolution of the semiconductor industry along Moore’s Law;

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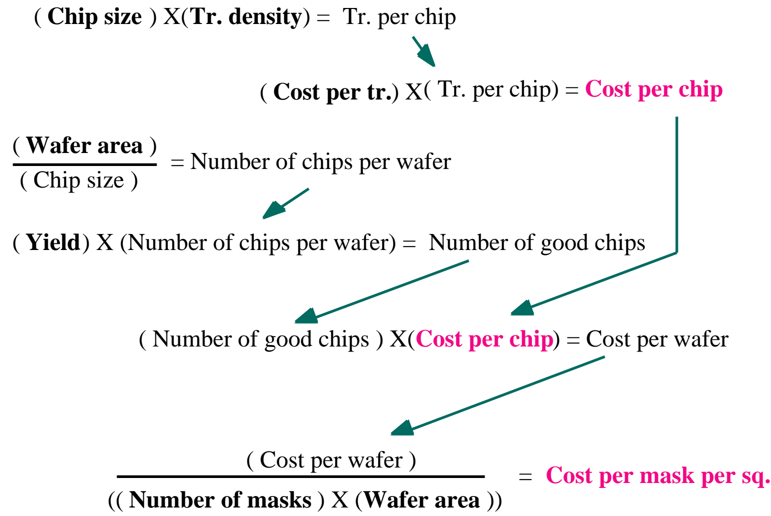
# SIA Road Map: Implications

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# SIA Road Map : MEMORY

| Year | 1995 | 1998 | 2001 | 2004 | 2007 | 2010 |
|---|---|---|---|---|---|---|
| Feature size [μm] | **0.35** | **0.25** | **0.18** | **0.12** | **0.1** | **0.08** |
| Tr. per chip [$10^6$] | **64** | **256** | **1024** | **4096** | **16384** | **65536** |
| Cost per tr. [millicents] | **0.017** | **0.007** | **0.003** | **0.001** | **0.0005** | **0.0002** |
| Chip size [$mm^2$] | **190** | **280** | **420** | **640** | **960** | **1400** |
| Wafer diameter [mm] | **200** | **200** | **300** | **300** | **400** | **400** |
| Tr. density [$10^6$ # tr. / $cm^2$] | **34** | **91** | **244** | **640** | **1707** | **4681** |
| Yield [%] | **90** | **90** | **90** | **90** | **90** | **90** |
| Number of chips per wafer | 142 | 93 | 148 | 91 | 110 | 72 |
| Wafer area [$cm^2$] | 314 | 314 | 706.5 | 706.5 | 1256 | 1256 |
| Number of good chips | 127 | 83 | 133 | 81 | 99 | 64 |
| Cost per chip [$] | *10.88* | *17.92* | *30.72* | *40.96* | *81.92* | *131.07* |
| Cost per wafer [$] | 1382 | 1487 | 4086 | 3318 | 8110 | 8389 |
| Number of masks | 18 | 20 | 20 | 22 | 22 | 24 |
| Cost per mask per sq.[$/$cm^2$] | *0.24* | *0.24* | *0.29* | *0.21* | *0.29* | *0.28* |

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# SIA Road Map : μPROCESSOR

| Year | 1995 | 1998 | 2001 | 2004 | 2007 | 2010 |
|---|---|---|---|---|---|---|
| Feature size [μm] | **0.35** | **0.25** | **0.18** | **0.12** | **0.1** | **0.08** |
| Tr. per chip [$10^6$] | **10** | **21** | **46.8** | **107.5** | **260** | **558** |
| Cost per tr. [millicents] | **1** | **0.5** | **0.2** | **0.1** | **0.05** | **0.02** |
| Chip size [$mm^2$] | **250** | **300** | **360** | **430** | **520** | **620** |
| Wafer diameter [mm] | **200** | **200** | **300** | **300** | **400** | **400** |
| Tr. density [$10^6$ # tr. / $cm^2$] | **4** | **7** | **13** | **25** | **50** | **90** |
| Yield [%] | **90** | **90** | **90** | **90** | **90** | **90** |
| Number of chips per wafer | 104 | 89 | 168 | 140 | 211 | 177 |
| Wafer area [$cm^2$] | 314 | 314 | 706.5 | 706.5 | 1256 | 1256 |
| Number of good chips | 93 | 80 | 151 | 126 | 189 | 159 |
| Cost per chip [$] | *100* | *105* | *93.6* | *107.5* | *130* | *111.6* |
| Cost per wafer [$] | 9300 | 8400 | 14134 | 13545 | 24570 | 17744 |
| Number of masks | 18 | 22 | 22 | 24 | 24 | 26 |
| Cost per mask per sq.[$/$cm^2$] | *1.65* | *1.22* | *0.91* | *0.80* | *0.82* | *0.54* |

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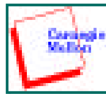
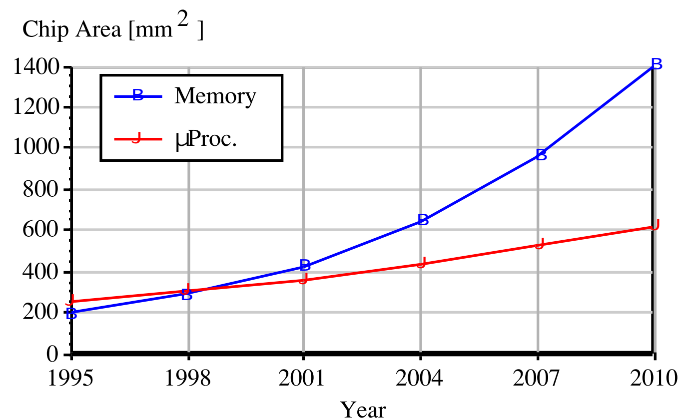


# SIA Road Map Assumptions - Chip Size

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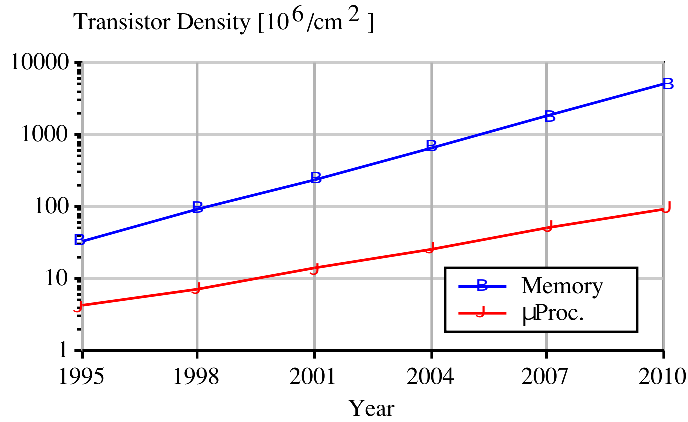
# SIA Road Map Assumptions - Transistor Density

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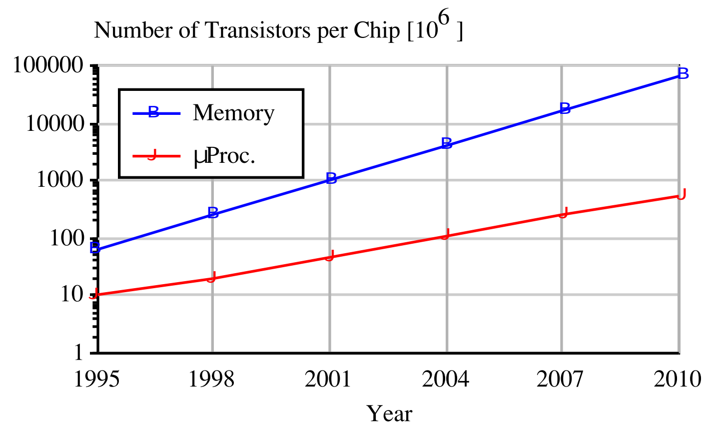
# SIA Road Map Consequences - Number of Transistors

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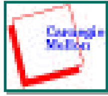
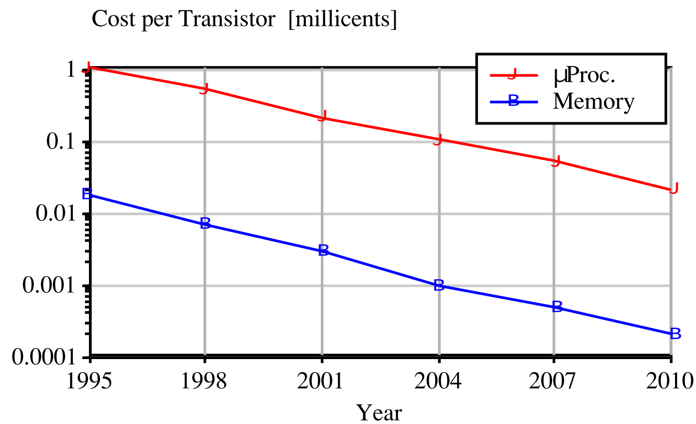



# SIA Road Map Assumptions - Cost

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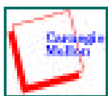
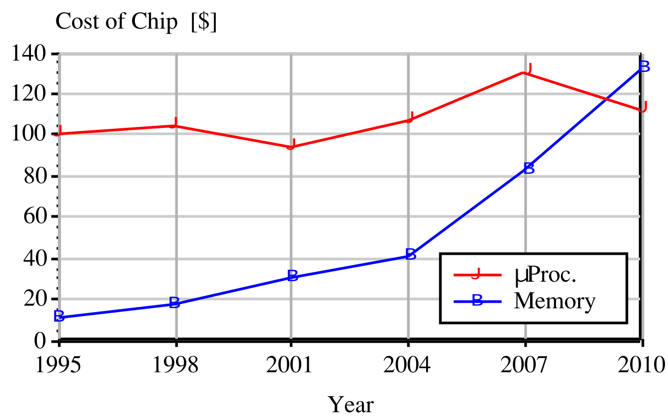



# SIA Road Map Consequences - Chip Cost

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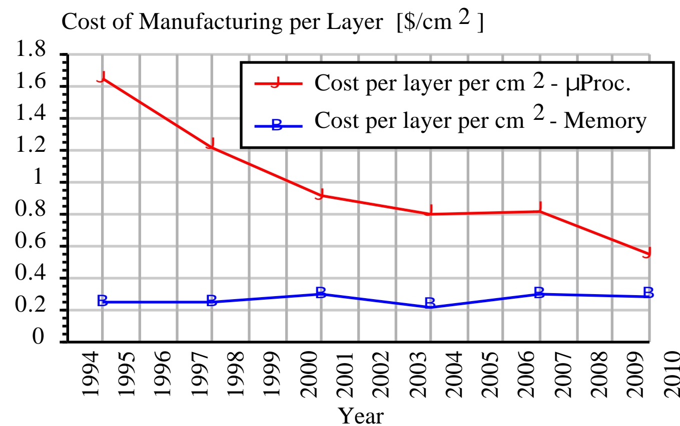
# SIA Road Map Consequences - Manufacturing Costs

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# SIA Road Map Consequences - Manufacturing Costs

**1994 SIA Road Map assumes that:**

- **exponential growth in die size,**
- **exponential growth in transistor density and**
- **exponential decrease in cost per transistor,**

**can be handled with unchanged (or even decreased) manufacturing cost per unit square.**

**Is such a goal really feasible ?**

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## Implications of SIA Road Map: Interconnect

| Year | Min. Feature Size [μm] | Interconnect Density [m/cm $^2$/level] | Interconnect Length [m] |
|---|---|---|---|
| 1995 | 0.40 | 35 | 380 |
| 1998 | 0.30 | 50 | 840 |
| 2001 | 0.22 | 70 | 2100 |
| 2004 | 0.15 | 105 | 4100 |
| 2007 | 0.11 | 125 | 6300 |
| 2010 | 0.08 | 155 | 10,000 |

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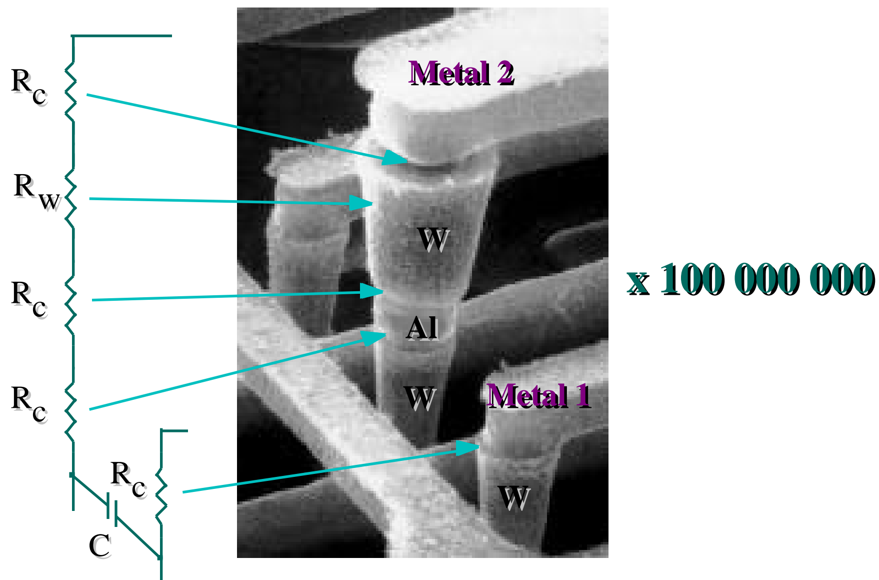
## Implications of SIA Road Map: Interconnect

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## Implications of SIA Road Map:
# Interconnect

Complexity of the interconnect will strongly affect the methodology of DESIGN, MANUFACTURING and TEST.

**Interconnect may become a main show stopper of the SIA Road Map.**

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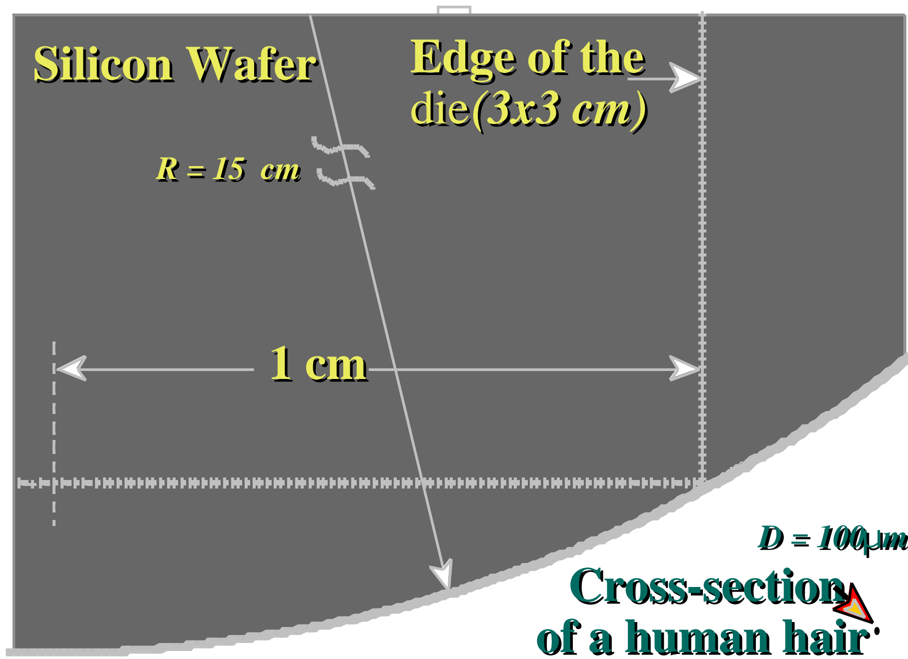


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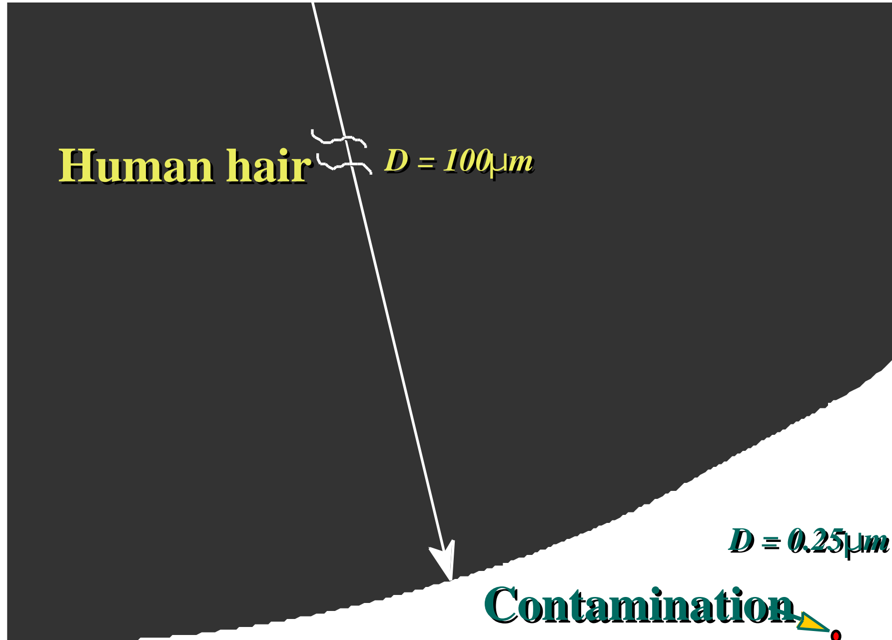
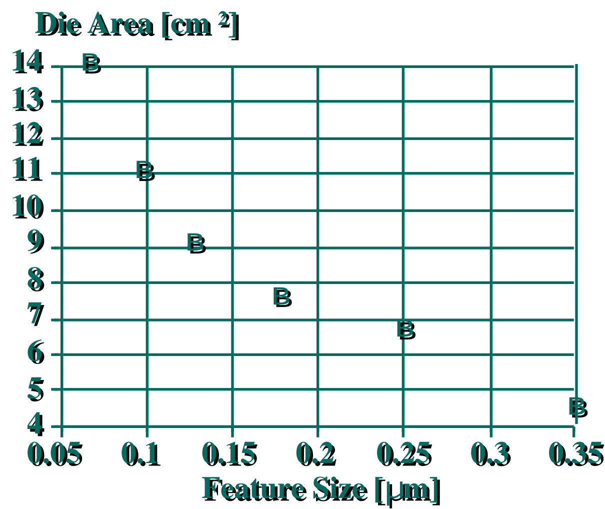





## Implications of SIA Road Map: Manufacturing



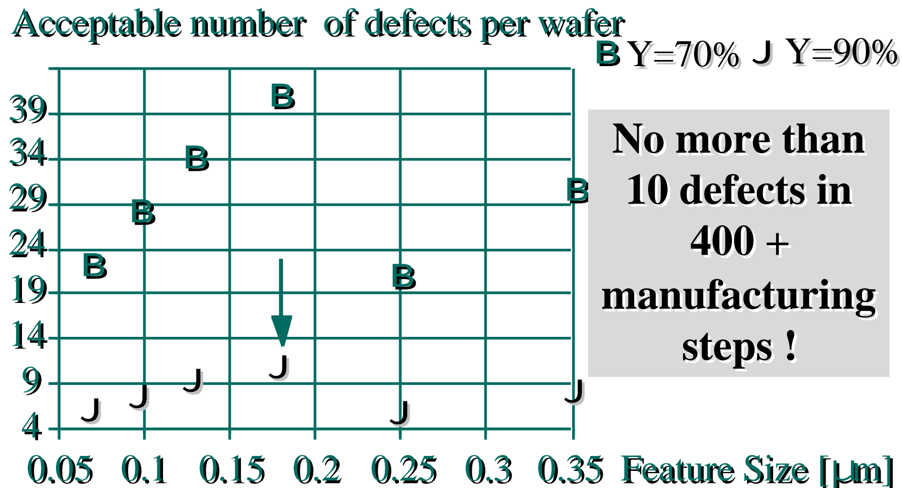

$$Y = \frac{1}{1 + A_{ch} D_0}$$

$$D_0 = \frac{1 - Y}{Y A_{ch}}$$

For Y = 70%
$D_0 = \frac{.43}{A_{ch}}$

For Y = 90%
$D_0 = \frac{.11}{A_{ch}}$

## Implications of SIA Road Map: Manufacturing

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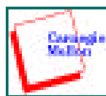


## Implications of SIA Road Map: Manufacturing

Complexity of IC processes must cause rapid increase in cost of IC manufacturing.

**Cost of manufacturing may become a main show stopper on the SIA Road Map.**

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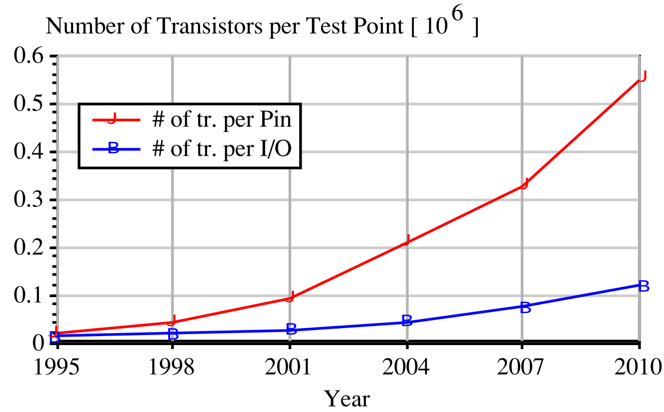
# SIA Road Map Consequences - Transistors per Test Point

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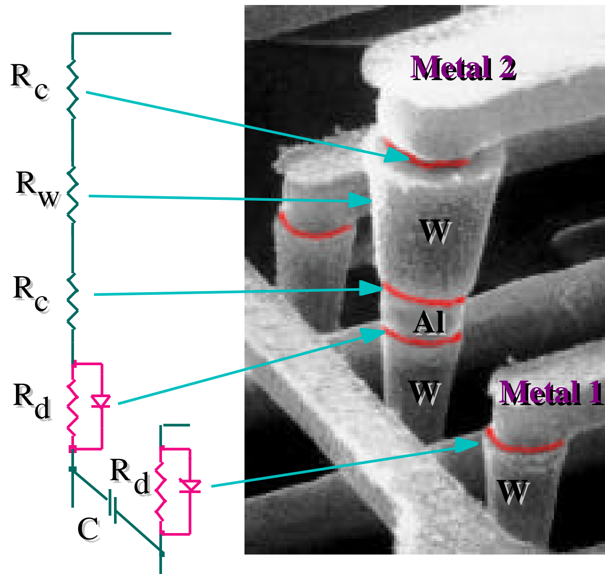
# Implications of SIA Road Map: Testing

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## Implications of SIA Road Map: Testing

- Testing will have to handle very large devices/ systems;
- New difficult-to-detect failures will have to be tested.
  - Data dependent cross-talk failures;
  - Power bus noise generated faults;
  - R-F coupling generated faults.
- Very high band-width testers will be required;
- **Massive application of DFT will be a must.**

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## Implications of SIA Road Map: Testing

Complexity of ICs to be tested will soon reach levels impossible to be handled with the testing paradigm as it is known today.

**Tester limitations may become a main show stopper on the SIA Road Map.**

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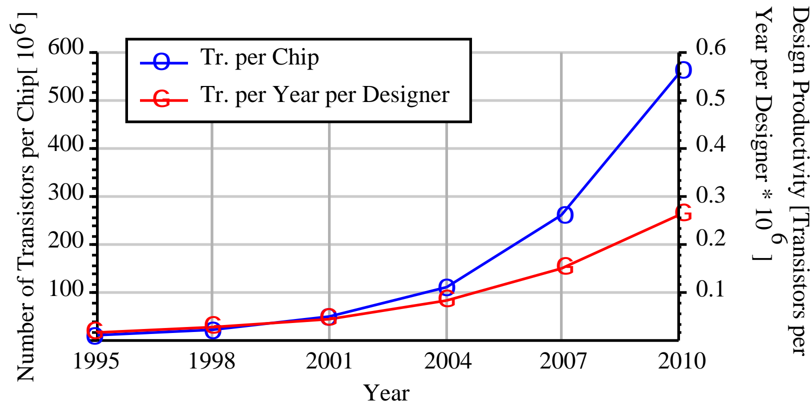
## Implications of SIA Road Map: Design




SEMATECH

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## Implications of SIA Road Map: Design

- **Design productivity will have to increase by orders of magnitude;**
- **Design verification (on all levels of design abstraction) will become an absolute necessity;**

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## Implications of SIA Road Map: Design

Size of ICs to be designed will soon reach levels impossible to be handled with the design paradigm as it is known today.

**Design productivity and design verification may become key show stoppers on the SIA Road Map.**

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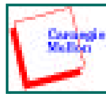


## SIA Road Map Consequences - Manufacturing Costs

1994 SIA Road Map assumes that

the substantial increase in complexity of :

- manufacturing,
- test and
- design,

can be handled with unchanged (or even decreased) manufacturing cost per unit square.

**Is such a goal really feasible ?**

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# SIA Road Map Consequences - Manufacturing Costs

1994 SIA Road Map assumes that
the substantial increase in complexity of :

- manufacturing,
- test and
- design,

can be handled with unchanged (or even decreased) manufacturing cost per unit square.

**Is such a goal really feasible ?**

**1997 Road Map says NO !**

*Cost of silicon will have to consume a rapidly increasing portion of the available profit margins.*

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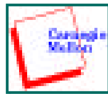
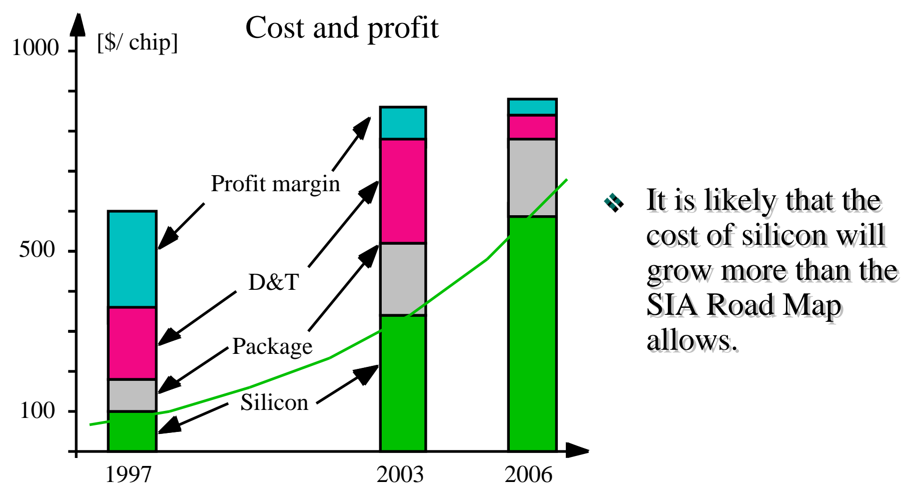


# SIA Road Map: Implications




- It is likely that the cost of silicon will grow more than the SIA Road Map allows.

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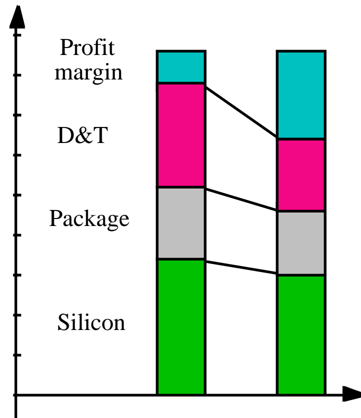
# SIA Road Map: Implications




$$C_{D\&T} = C_{TE} + \frac{C_D + C_{TG}}{V_{Ch}} \longrightarrow C_{TE}$$

- Cost of D&T can be substantially reduced by increasing volume of sold chips.

$$C_{Silicon} = C_{Material} + C_{Own.} + \frac{C_{TD}}{V_{Ch}}$$

- Cost of silicon cannot be reduced beyond a certain level by increasing volume of sold chips.

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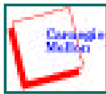
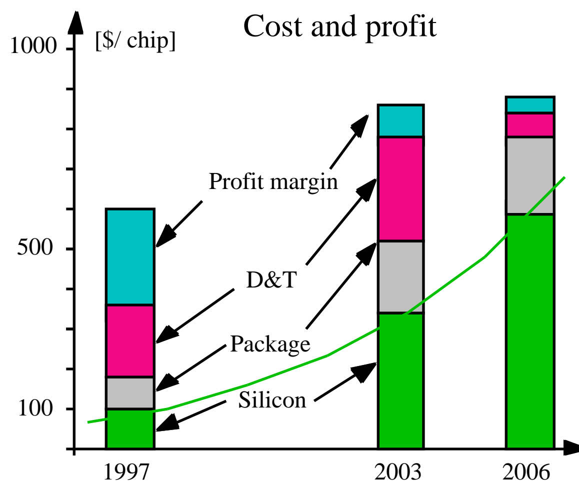



# SIA Road Map: Implications


- It is possible that the only market advantage for many IC producers will be achievable via high efficiency and high quality design and test;

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# Design Quality

| | **Intel P6 ( Kalmath)** | **Mitsubishi D30V** |
|---|---|---|
| Type: | CISC (32 bit data/instr.) | DSP LIW (64 bit instr.) |
| Applications: | Universal (MPEG2, ...) | M-Media (MPEG2, V-ph.) |
| Load for DVD: | 100 % | 90 % |
| Technology: | 0.28 μm CMOS | 0.3 μm CMOS |
| Clock: | 233 MHz; | 250 MHz; |
| # Trans. Total: | 7.5 M (with 32K L1 cache) | 300 K + 64K SRAM |
| Area: | 203 $mm^2$ | 37 $mm^2$ |
| Price: | TBA | TBA |
| | (PPro - 200 MHz = $1072) | (Est. < $50) |

Compiled by **Pierre Paulin** of ST based on the data published in EE Times and μP Rep.

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# SIA Road Map Implications

SIA Road Map will cause:

- **Cost of silicon to go up;**
- **Price of chips to go up (but with well defined upper limit);**
- **Progress along Moore's curve to slow down;**
- **Design and test budgets to go down;**
- **Design efficiency and design quality to become the most important knobs in profit maximization.**

*New and very efficient design strategies capable of producing very high **QUALITY IC DESIGNS** will eventually became **the key enablers** of the SIA Road Map vision.*

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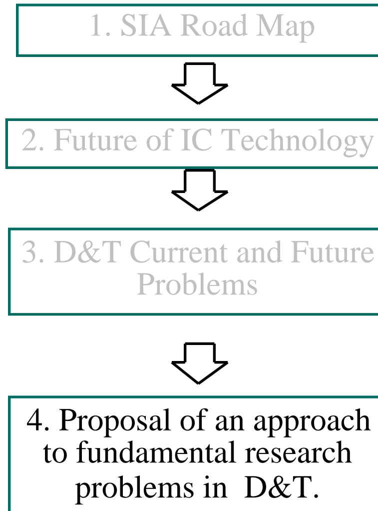
# Outline




4. Proposal of an approach to fundamental research problems in D&T.

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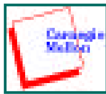
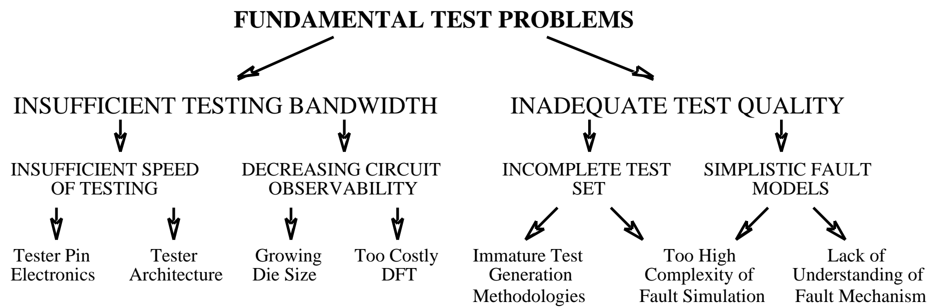


# Fundamental Problems: TEST

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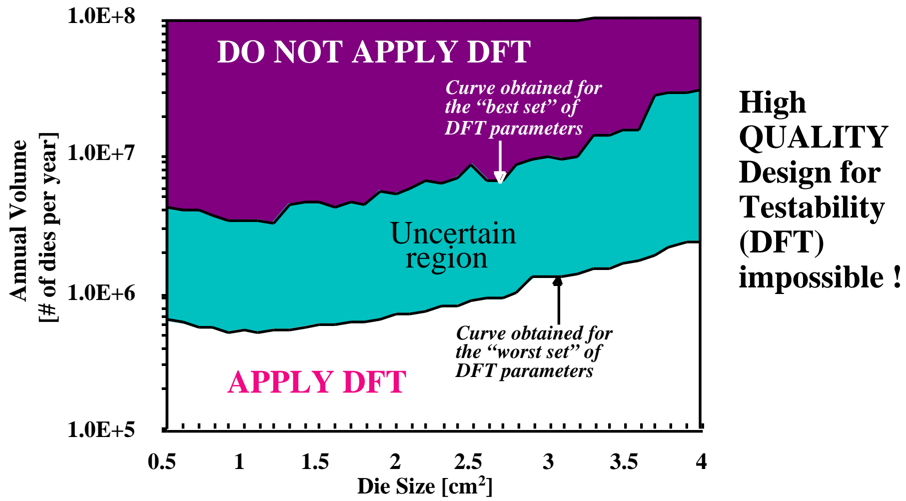
# Fundamental Test Problem




**High QUALITY Design for Testability (DFT) impossible !**

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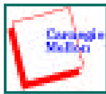
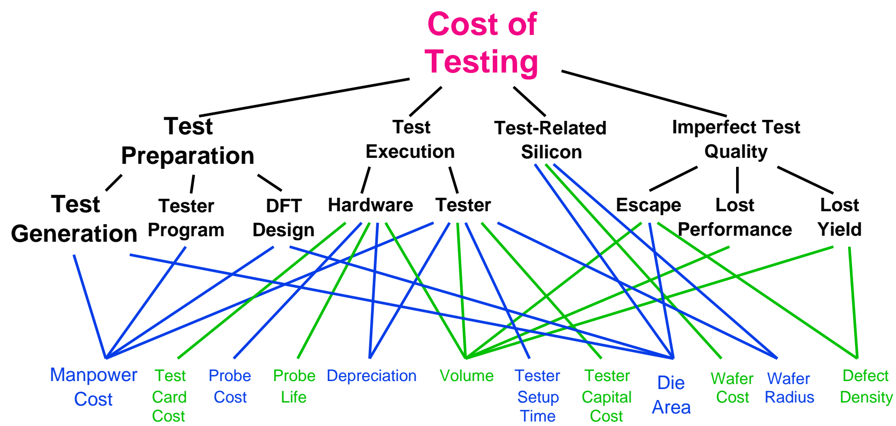


# Fundamental Test Problem

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# Fundamental Test Problem

$$C_{prep} = C_{test_gen} + C_{test_prog} + C_{design_of_DFT}$$

$$C_{design_of_DFT} \rightarrow 0$$

$$C_{test_gen} = \frac{\boldsymbol{R}_{\boldsymbol{man_hour}} T_{test_gen}}{\boldsymbol{V}}$$

$$T_{test_gen} = \boldsymbol{K}_{\boldsymbol{test_gen}} e^{A_0} \rightarrow C_{test_prog} = {}_{\boldsymbol{test_prog}} C_{test_gen}$$

*Examples of FUNDAMENTAL test problems:*

- Lack of the theory bridging the gap between circuit design decisions and test generation complexity.
- Superficial understanding of delay testing needs and principles.
- ..........................................................................................................

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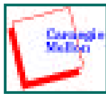
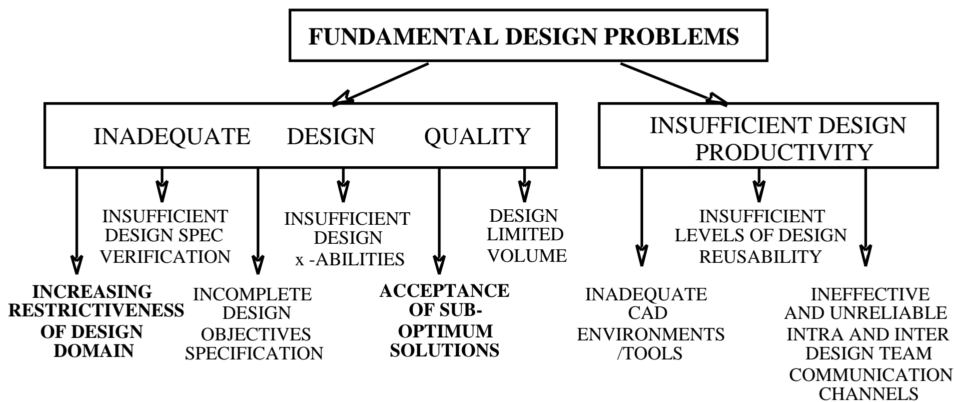


# Fundamental Problems: DESIGN

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## Limitations of Design Domain

$R_c$
$R_w$
$R_c$
$R_c$
$R_c$
C

Metal 2
Metal 1

**x 100 000 000**

*Example of a FUNDAMENTAL CAD problem:*

Lack of adequate design data base which:

- Allows to model all timing relevant interconnect geometry details;
- Enables efficient parasitic extraction in VERY large circuits;
- ..........................

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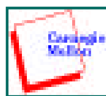


## Sub-optimum Designs

| Intel P6 ( Kalmath) | Mitsubishi D30V |
|---|---|
| CISC (32 bit data/instr.) | DSP LIW (64 bit instr.) |
| MPEG2 | MPEG2 |
| 7.5 M (with 32K L1 cache) | 300 K + 64K SRAM |
| 203 $mm^2$ | 37 $mm^2$ |

*Is Mitsubishi design close enough to optimum ?*

*Example of a FUNDAMENTAL design problem:*

Lack of adequate objective functions for hardware-software co-design which :

- Take into account cost and time of design process;
- Forecast volume to be sold;
- Predict true cost of manufacturing.

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# Conclusions

- Microelectronics industry may approach a high-cost-of-manufacturing-based crisis;
- Design&Test may need to:
  - operate with lower time and “$” budgets;
  - become a main and the only provider of market advantage;
  - deliver much **better** designs.
- Design&Test community need to re-think the traditional view on its role and strategy;

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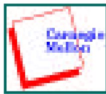
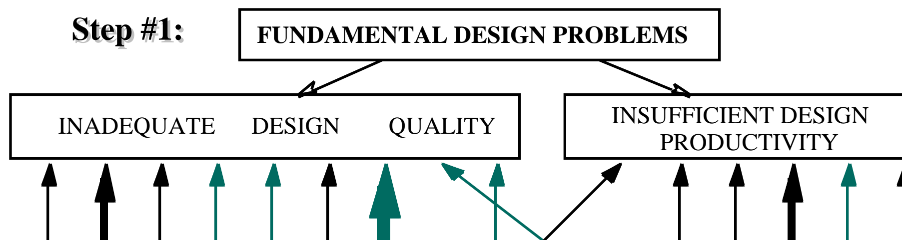


# Conclusions

**D&T Research Strategy Proposal**

- Community-wide collaboration;
- Consensus on the initial “Vision”.
- SIA Focus Center ?
- Multi-disciplinary cross-domain approaches;

**Step #1:**

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