A Point of View on the Future of IC Design, Testing and Manufacturing

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Invited*

For at least last 30 years microelectronics has been evolving rapidly tracking - almost without a single deviation - Moore's Law [3]. Such spectacular progress has been driven by the development of better technologies using constantly improved, but also more expensive, manufacturing equipment. Design and test have followed, struggling with technology-enabled performance opportunities and technology-generated complexity.

At the beginning of nineteen nineties some level of concern was expressed whether continuing along Moore's prediction makes economic sense. The main reason for such concern has a source in exponentially growing cost of manufacturing equipment [4]. The costs of design and testing have also been identified as growing with a rate too high to be ignored.

Despite growing costs of manufacturing in 1993 and 1994 the Semiconductor Industry Association (SIA) has proposed "The National Technology Roadmap for Semiconductors", focused on the farther decreases of the transistors minimum feature size. This Roadmap (which is also referred to as the "SIA Roadmap") proposes an aggressive schedule of milestones to be achieved by the semiconductor industry in next 15 years [5]. The true motivation of the SIA Roadmap seems to be, however, a consolidation of the entire semiconductor industry on a single set of coherent goals. Such a consolidation has been perhaps seen as a necessary step in focusing industry government and universities on the same technology development objectives. Unification of the objectives could be the most effective way to build momentum which should allow the equipment industry to meet all the challenges of subsequent submicron technologies. Hence, from such a perspective one can see the SIA Roadmap as a "self-fulfilling prophecy" which facilitates continuation of the evolution of semiconductor industry along the Moore's Law. It should also be seen as an agenda focused on achieving ever smaller transistor sizes with ever more complex and, unfortunately, ever more expensive manufacturing processes.

There are a number of indicators suggesting that the SIA Roadmap has begun to materialize. For instance, Intel's impressive manufacturing accomplishments [6] seem to confirm the feasibility of the first few milestones of the Roadmap. Such opinion must be shared by all key semiconductor players who have announced plans [7] to build high volume, 200 mm, sub 0.5 μm fablines. (Dataquest predicts [8] that by the year 2000 around 200 new fablines will be built.) Without much exaggeration one can conclude, therefore, that the SIA Roadmap has decided the near future for the entire electronics industry.

There are a number of very important implications of both the ambitious goals of the SIA Roadmap and the way these goals have been established. The most important of them are derivatives of a timely-

* This paper is a summary of key points of two talks given by the author at: [1] European Design and Test Conference 1996 and [2] International Test Conference 1996.

decrease-of-transistor-feature-size as primary goal of the Roadmap and strong focus on equipment-for-smaller-transistor related issues. Consequences of these two Roadmap's characteristics will have a strong and not only positive impact on manufacturing, testing and design. This summary discusses some of them in more detail.

Year	Min. Feature Size [μm]	Die Size [cm ^{2}]	# of I/Os	Freq. [MHz]	Dens. [tr./ cm ^{2}]	# of Tr. [mln]
1995	0.35	2.5	512	300	4.0E+6	10
1998	0.25	3	512	450	7.0E+6	21
2001	0.18	3.6	512	600	1.0E+7	47
2004	0.13	4.3	512	800	2.0E+7	107
2007	0.1	5.2	800	1000	5.0E+7	290
2010	0.07	6.3	1024	1100	9.0E+7	558

Table 1.

Year	Min. Feature Size [μm]	Interconnect Density [m/cm ^{2}/level]	Interconnect Lenght [m]
1995	0.40	35	380
1998	0.30	50	840
2001	0.22	70	2100
2004	0.15	105	4100
2007	0.11	125	6300
2010	0.08	155	10,000

Table 2.

To provide a background for such discussion it is useful to begin with a summary of SIA Roadmap objectives. A few key objectives are listed in Table 1. The proposed milestones and resulting IC characteristics seem to be a natural extension of the trends known from the past. But the level of difficulty of the Roadmap's implementation cannot be fully recognized unless crucial details of the Roadmap implementation are considered. Table 2 summarizes, for instance, a derivative of the Roadmap objectives extrapolated the onto the interconnect arena. To stress the difficulty of implementing the interconnect portion of the SIA Roadmap [9], Fig. 1 shows a small segment of interconnect of PowerPC 603 microprocessor fabricated with 0.65 μm minimum feature size and 4 metal layers (only two of them are shown in Fig. 1.)

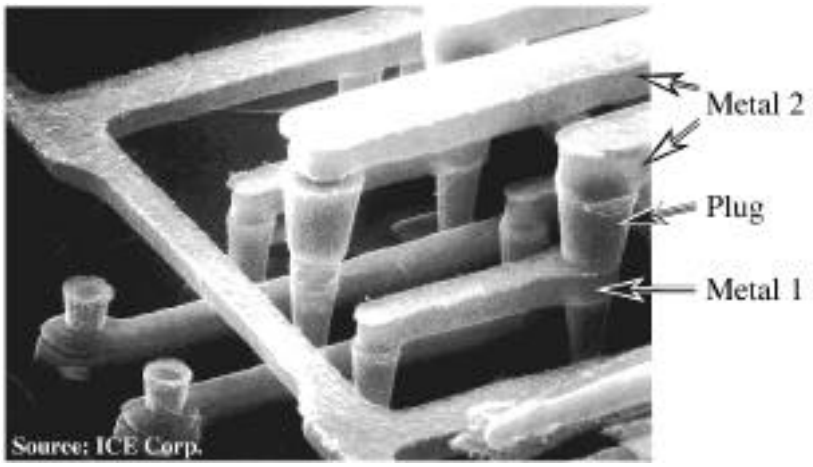

Figure 1. Small segment of interconnect of PowerPC 603 (Source ICE Corp.).

The proximity of individual interconnect elements and true 3-D nature of the shown structure could be good indicators of the complexity of an IC device, for instance, with 6 to 7 metal layers and total

interconnect length in the range of 4 km. It also underscores the complexity of the design, testing and manufacturing tasks which will have to deal with, on one hand, the enormous size of the circuit and, on the other hand, with every detail of the interconnect geometry and three-dimensional electrical interaction between the circuit's nodes.

Further illustration of the implementation complexity of the SIA Roadmap is given in Figs 2 and 3. Fig. 2 indicates some of testing related implications of the Roadmap's objectives. It shows a testing difficulty index, defined as a ratio of number of transistors to the number of I/Os, for subsequent Roadmap milestones. Fig. 3 describes the maximum acceptable level of contamination per manufacturing wafer. Observe that the expected level to be achieved in five years translates into requirements of less than 1 contamination deposited on the water of the frisbee size per layer when a harmful contamination is assumed to be any particle larger than only 600 A.

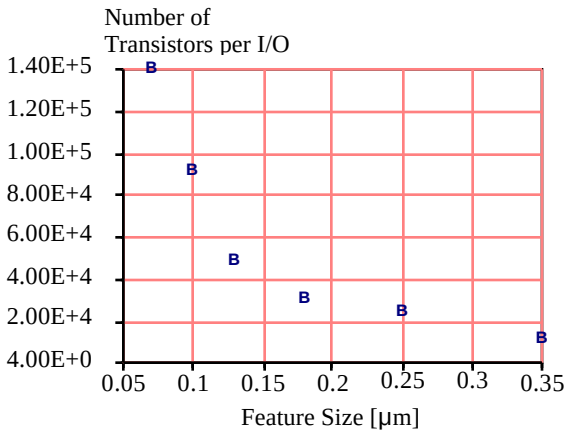

Figure 2.

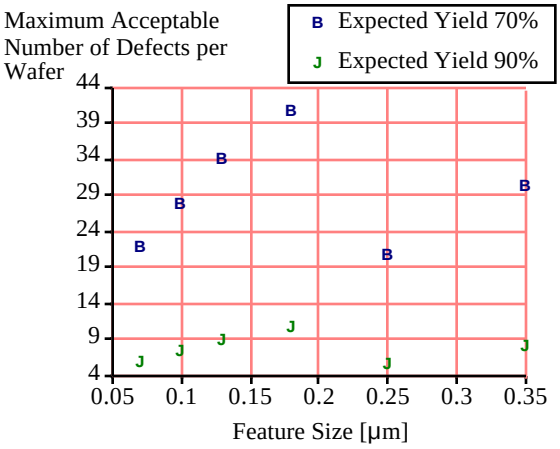

Figure 3.

The above indicators are by no means adequate for forecasting the future trends in manufacturing, design or testing. But they can be used to predict which of the directions of current development trends may be dead-end streets and which new directions we will have to focus on. For instance, for the testing domain one can conclude that:

a. Current testing equipment evolution cannot be continued and very soon will have to be dramatically modified. Simply one cannot imagine that by building more expensive version of current testers one can meet the testing requirement of 100 million transistors tested through 2000 pins and 800 MHz clock [10]

b. DFT and BIST are the only direction testing can take even if one can still hear prominent opposition [11] to the concept of using extra silicon for testing purposes* .

c. Non-traditional kinds of IC "misbehaviors" will have to be handled. Delay faults are among them. More complicated faults such as data dependent cross-talk based "temporary bridges" (see again Fig. 1) or power bus and substrate generated noise based faults will have to be modeled and detected.

d. Testing, as the only true source of information about process quality, will have to be used for process and design debugging. This means that such tasks as fault diagnosis or localization of "invisible" defects in multimillion transistors circuits will have to be performed quickly on a volume of fabricated devices.

This short and incomplete list of future challenges raises a very important question: Are we ready to undertake them in an adequate manner ? Of course, one cannot answer "No" but it is useful to list a couple of problems which may become important show stoppers. Focusing again on testing one can claim that:

a. The testing equipment industry seems to be too small to undertake the necessary research and development steps by itself to allow for a for dramatic departure from today's "Supercomputer" status of testing hardware.

b. Inadequate status of "testing economy" component in the strategic design/manufacturing decision making process generates unjustified opinions about cost /benefits of DFT and BIST.

c. Traditional roots of testing theory still constrain the testing domain to levels of abstraction remote from the physical phenomena which actually cause IC failures.

d. Testing research is focused on solvable problems, useful mainly for publication purposes, staying away from some crucial and intellectually very challenging problems. At the same time industrial practitioners guard essential information for themselves instead of educating researchers about real problems to be solved.

e. Testing is viewed as a service by the design community which at the same time is not willing to help with manufacturing tasks such as process debugging.

Of course, there are a number of exceptions contradicting the above statements. One must conclude, however, even based on the above examples, that testing, as well as design and manufacturing, are unlikely to be able to overcome the difficulties posed by the SIA Roadmap -- as long as the solutions are sought within each individual domain. For instance, the signal integrity problem, generated by the density and complexity of the interconnect, cannot be solved within the design domain itself unless some form of, for instance, extra shielding is provided by manufacturing. (Manufacturing for Designability!) Manufacturing will not be able to achieve the desired contamination levels unless design and testing enable fast failure analysis. (Need for Design for Failure Analysis - DFFA!). And testing cannot address the delay testing bottleneck unless design will accept the fact that testing is a design problem which must cost extra silicon and extra design time (as well as new ideas, for example, for on-chip delay testing!).

Figures 4 and 5 generalize the above observation. Figure 4 summarizes key problems of design, manufacturing and testing. Design productivity and verification are the two key problems of VLSI

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* In his ITC-95 Keynote Ken Thompson, Intel's, V.P. of Manufacturing argued that: "1% area increase for DFT means $63 million/year" of extra cost and that "15% area increase would require $1 billion more in fabrication capacity for the

design. The productivity problem almost certainly will have to be addressed by the design reuse and the design migration supported by some form of intellectual property (IP) exchange mechanism. It is likely that such exchange, enabled by exhaustive characterization of reused (migrated) entities, will have to be done using manufacturing silicon houses as a base. Design verification, especially on the physical levels of design abstraction, will require process level solutions. The key manufacturing problem is, and will be, cost. Here, in addition to process simplifications and efficient manufacturing, rapid yield learning will play an important cost improvement rule. But rapid yield learning will require fast feed-back from the product obtained via interpretation of the test results. Finally, testing will have to address to major issues: tester band-width problem and testing quality problems. Both will have to be solved in close collaboration with design and manufacturing.

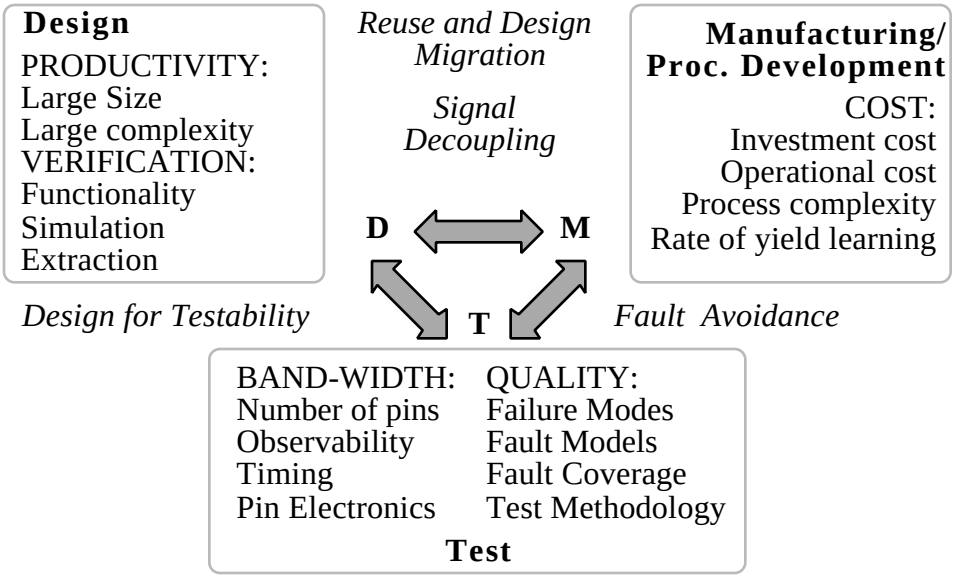

Figure 4. Key issues on the "roadmap" to the SIA Roadmap.

In general one must conclude that the progress planned by the SIA Roadmap requires much closer interaction between design testing and manufacturing. This interaction seems likely to evolve in the way suggested by Fig. 5. Namely, it is likely that band-width related testing problems will be solved by the design domain. The design productivity problems will be solved (or at least addressed) by manufacturing domain which will provide fully characterized, manufacturable and testable design macros. Finally, manufacturing domain will be assisted by testing in process/design debugging.

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same number of products".

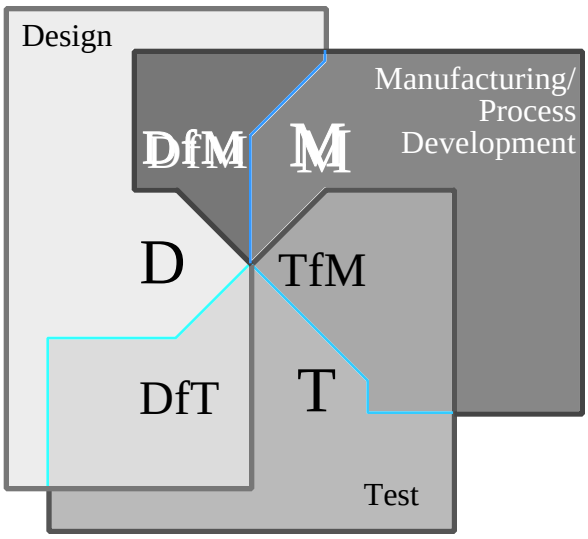

Figure 5. Close collaboration between design, test and manufacturing.

In the other words, future of the SIA Roadmap depends on our ability to develop Design for Manufacturabilit (DfM), Design for Testability (DfT) and Test for Manufacturability (TfM) domains.. Such developments require that experts of each domain learn how to seek potential solutions of the problems posed by the inherent progress of technology, outside of the their own domains. And the rate of our learning -- not the SIA Roadmap itself -- will decide what will be the ultimate rate of the decrease of the minimum feature size.

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