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Harris Real Time Express:
A New Concept for Realtime Control

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Agenda - Rochester RTX Seminar

o	Introduction/ Technology overview	Auditorium
o	RTX 2000 Architecture	Auditorium
o	RTX Applications & Interfacing	Auditorium
o	RTXDS Background	Auditorium
o	Lunch	
o	Guest Speakers	Auditorium
o	RTXDB	May Room
o	TForth Compiler & Utilities	May Room
o	Debugger	May Room

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RTX 2000 ARCHITECTURE

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RTX 2000 ARCHITECTURE

- BASED ON NOVIX 4016/6016 ARCHITECTURE
- ON-CHIP PARAMETER AND RETURN STACKS
- ON-CHIP PERIPHERALS
  - MULTIPLIER
  - INTERRUPT CONTROLLER
  - COUNTER/TIMERS
- ADDRESS 1 MEGABYTE OF MEMORY

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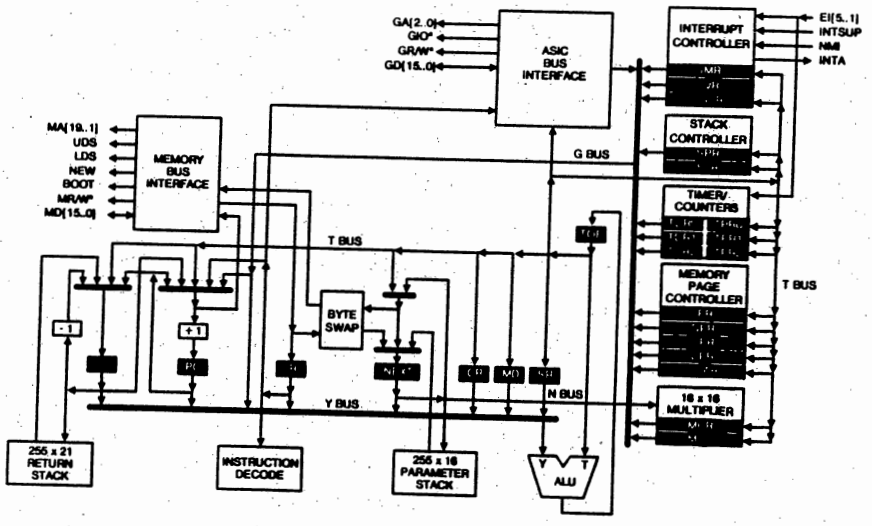
RTX 2000 Block Diagram



Stacks

- **Parameter Stack**
  - 256 words deep
  - 16 bits wide
  - Top two elements are available through on-chip registers
- **Return Stack**
  - 256 words deep
  - 21 bits wide
    - 15 bits Program Counter
    - 4 bits Code Page
    - 1 bit interrupt status
    - 1 bit Data Page flag
  - Top element available through on-chip register

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Registers

- Top - top element of Parameter stack
- Next - second element of Parameter stack
- Index - top element of Return stack. Loop counter.
- Control/Status
  Configuration Register (CR)
  Interrupt Base/Control Register (IBC)
- Multistep Divide (MD) - used for step math or general purpose
- Square Root (SR) - used for square roots or general purpose
- Memory Page registers
  Code Page - instruction fetches
  Data Page - memory access (@ ! etc)
  User Page - user memory access
- I/O devices
  Multiplier output
  Counter/timers
  Interrupt mask
  Interrupt vector
  Stack pointers
  Stack limits

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On-Chip Peripherals

- Stack Controllers
  Programmable limit registers
  Generate interrupts on overflow and underflow conditions
- Interrupt Controller
  14 interrupt sources, internal and external
  13 maskable, 1 non-maskable
  Software interrupt
- Multiplier
  Single cycle 16 x 16 multiply with 32-bit result
  Forth * in 3 cycles
- Counter/Timers (3)
  16-bit down counters
  Clocked internally (timers) or externally (counters)
  Generate Interrupts on 0 count

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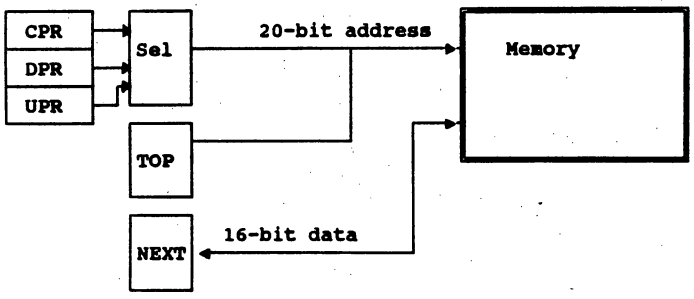
Memory Interface

- 1 Megabyte address space
  16 32K pages
- Page registers select appropriate page
- Byte and Word access

Memory Interface



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ASIC Bus™

- Data path between Top and other registers and I/O devices
- Input data is fed through ALU before going into Top
- Simple interface for multi-RTX applications

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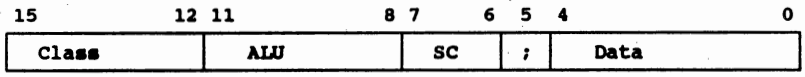
RTX Instruction Set

All processor instructions are 16 bits, with the following general fields:



Class - General type of instruction:
- Subroutine call
- Branches and loops
- Math/Logic functions
- Register and I/O access
- Short literal
- Long literals
- Main memory access
- User memory access

ALU - ALU function to be performed.

SC - Subclass. Function depends on Class field.

; - Return bit. When set, causes a Return-from-subroutine

Data - depending on Class, indicates shift operation, short literal data, G-space address, or memory address.

RTX Instruction Set

Subroutine Calls
- Subroutine call takes place in one clock cycle
- Return-from-subroutine can be part of another instruction

Branching and Looping
- Unconditional branch
- Conditional branch based on contents of Top register
- Conditional branch based on contents of Index register with auto decrement of Index register

ALU Operations
+ - SWAP- AND OR NAND NOR XOR XNOR NOT

Shift Operations
- 16 and 32-bit shifts, either direction
- Signed and unsigned shifts
- Can be combined with ALU operations

Step Math
- Divide
- square root

Register-I/O Access
- Read/write processor register or I/O device
- Combine ALU operation with data from register

Short Literals
- Load value 0 - 31 into Top register
- Combine ALU operation with data
- Literal value is embedded in instruction

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RTX Instruction Set

Long Literals
- Load 16-bit value into Top register
- Combine ALU operation with data

Memory Access
- Address in Top register, data in Next register
- Access memory by byte or by word
- Access program memory, data memory, or user memory
- Access memory in either MSB-LSB or LSB-MSB byte order
- Combine ALU operation with memory data
- Move blocks of memory to/from stack with auto address update

Streamed Instruction Mode
- Execute instruction repeatedly without extra fetch cycles

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HARRIS RTX2000 PROCESSOR PINOUT

MEMORY INTERFACE PINS

ASIC BUS INTERFACE PINS

INTERRUPT / RESET PINS

CLOCK / WAIT PINS

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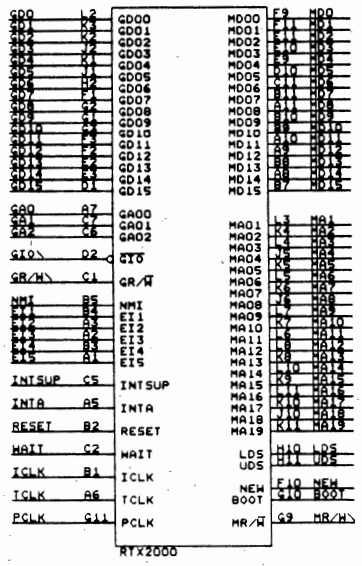
HARRIS RTX2000

INTERFACING THE RTX2000: PROCESSOR PINOUT



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HARRIS RTX2000 MEMORY INTERFACE PINS

MD00 TO MD15: MEMORY DATA BUS

MA01 TO MA19: MEMORY ADDRESS BUS

LDS, UDS: LOWER / UPPER

DATA SELECT (NOT STROBED)

NEW: INSTRUCTION FETCH

BOOT: GENERAL PURPOSE

MR/W\: MEMORY READ / WRITE

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HARRIS RTX2000 ASIC BUS INTERFACE PINS

GD0 -GD15: G-BUS DATA

GA0 - GA2: G-BUS ADDRESS

GIO\: G-BUS STROBE

GR/W\: G-BUS READ/WRITE\

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INTERRUPT/RESET PINS

NMI: NON-MASKABLE INTERRUPT
EI1 - EI5: EXTERNAL INTERRUPTS
EI3 - EI5: TIMER/COUNTER INPUTS
INTSUP: INTERRUPT SUPPRESS
INTA: INTERRUPT ACKNOWLEDGE
RESET: MASTER RESET

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CLOCK/WAIT PINS

WAIT: WAIT STATE INPUT
ICLK: INPUT CLOCK
TCLK: TIMING CLOCK
FREE RUNNING
PCLK: PROCESSOR CLOCK
HELD LOW FOR WAIT STATES

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MINIMAL SYSTEM TIMING

ALLOWS THE USE OF THE SLOWEST MEMORIES NO DECODE OR BUFFERING IN ADDRESS OR CHIP ENABLE PATHS AT MAX SPEED: WE\ DELAYED TO ASSURE ADDRESS SETUP TIME TAA = TCY - TAV - TRDS

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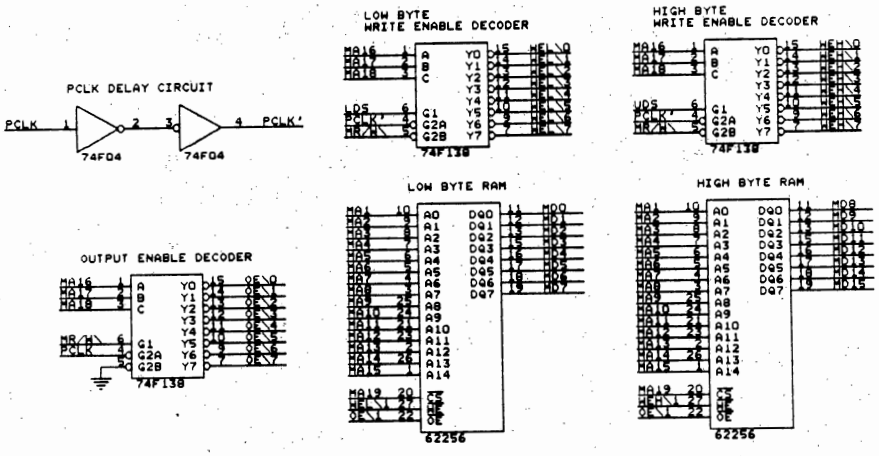
INTERFACING TO RAMS: MINIMAL SYSTEM



CRITICAL SPEED PATH: USUALLY ADDRESS ACCESS TIME

TAA = TCY - TAV - TRDS

	10MHz	8MHz
TCY: PCLK CYCLE TIME	100	125
TAV: PCLK HIGH TO ADDRESS VALID	53	56
TRDS: READ DATA VALID TO PCLK HIGH	12	12
TAA: MEMORY ADDRESS ACCESS TIME	35	57

NOTE:
FOR SPEEDS ABOVE 8MHz, WE\ IS GATED WITH DELAYED PCLK: PCLK'.
AT 8MHz AND BELOW, GATING WITH UNDELAYED PCLK IS SUFFICIENT.

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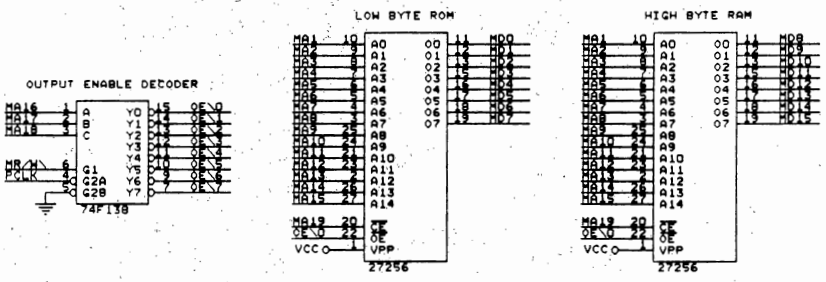
INTERFACING TO ROMS: MINIMAL SYSTEM



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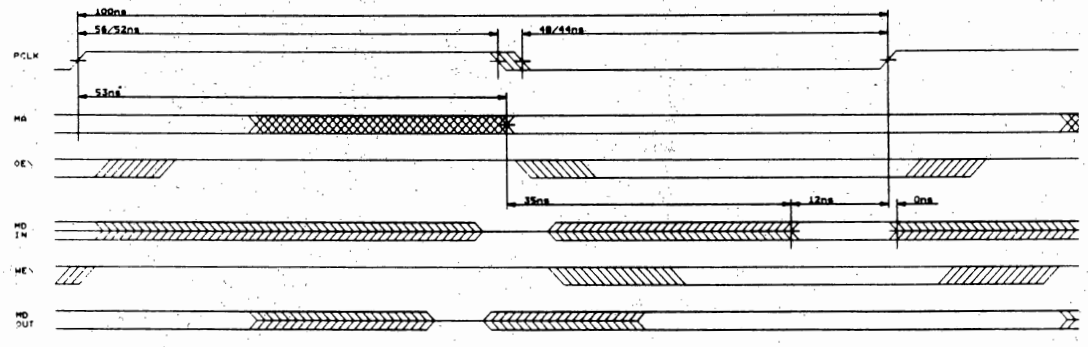
MINIMUM SYSTEM: 10MHz TIMING



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HARRIS RTX2000
UNBUFFERED SYSTEM TIMING

ALLOWS GREATER DECODING RANGE
LOWER SYSTEM POWER
ONLY ONE DECODER IN CRITICAL PATH
TAA = TCY - TAV - TPD - TRDS
WE\ REQUIRES GREATER DELAY AT FULL SPEED

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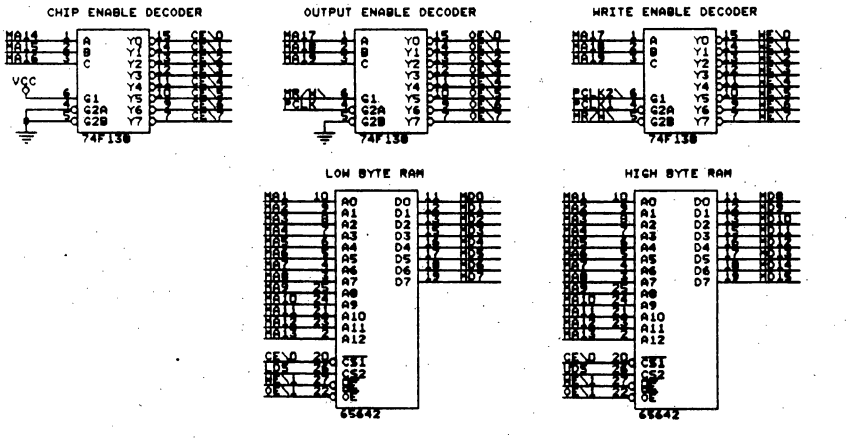
HARRIS RTX2000

INTERFACING TO RAMS: UNBUFFERED SYSTEM



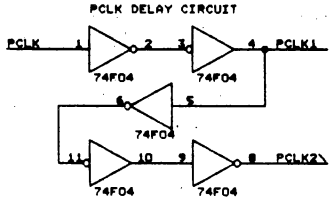
CRITICAL SPEED PATH: USUALLY CHIP ENABLE ACCESS TIME

TAA = TCY - TAV - TPD - TRDS

PARAMETER	10MHz	8MHz
TCY: PCLK CYCLE TIME	100ns	125ns
TAV: PCLK HIGH TO ADDRESS VALID	53ns	56ns
TPD: 74F138 PROP DELAY TIME	8ns	8ns
TRDS: READ DATA VALID TO PCLK HIGH	12ns	12ns
TAA: MEMORY ADDRESS ACCESS TIME	27ns	49ns

NOTE:
ADDRESS MAY BE BUFFERED ONE LEVEL WITHOUT A SPEED PENALTY.
WRITE ENABLE MAY BE GATED WITH UNDELAYED PCLK WHEN FREQUENCY IS LESS THAN OR EQUAL TO 8MHz.

PCLK DELAY CIRCUIT



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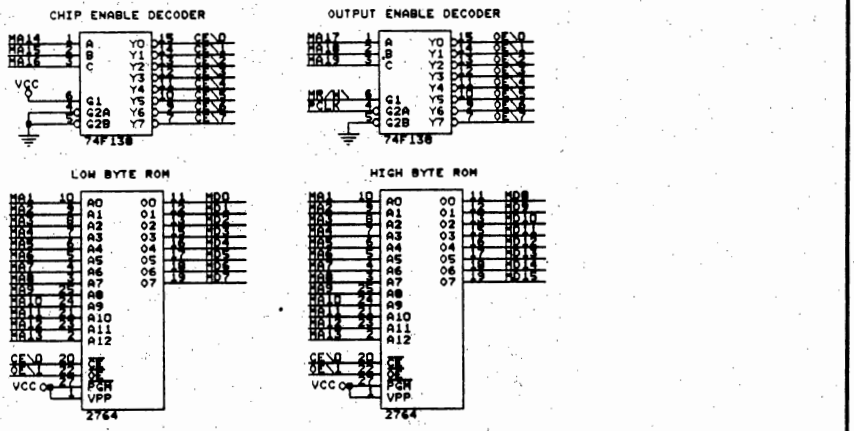
HARRIS RTX2000

INTERFACING TO ROMS: UNBUFFERED SYSTEM



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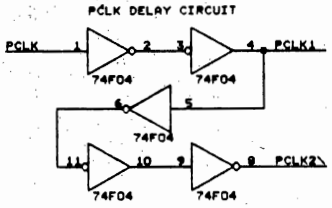

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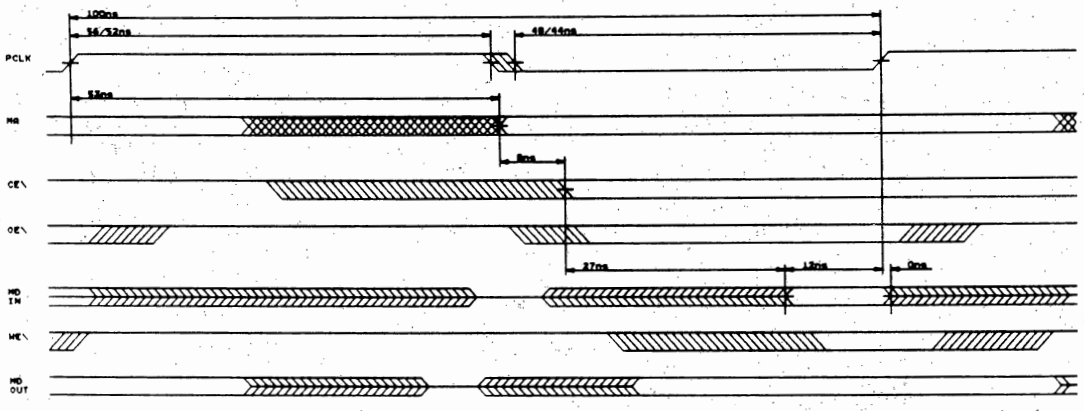
UNBUFFERED SYSTEM: 10MHz TIMING



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HARRIS RTX2000 BUFFERED SYSTEM TIMING

FULLY BUFFERED FOR LARGE MEMORY ARRAYS

DATA BUFFER DELAY IN CRITICAL SPEED PATH

BOTH WE\ AND DATA BUFFER ENABLE DELAYED FOR WRITE CYCLE AT FULL SPEED

TAA = TCY -TAV -TDD - TBD -TRDS

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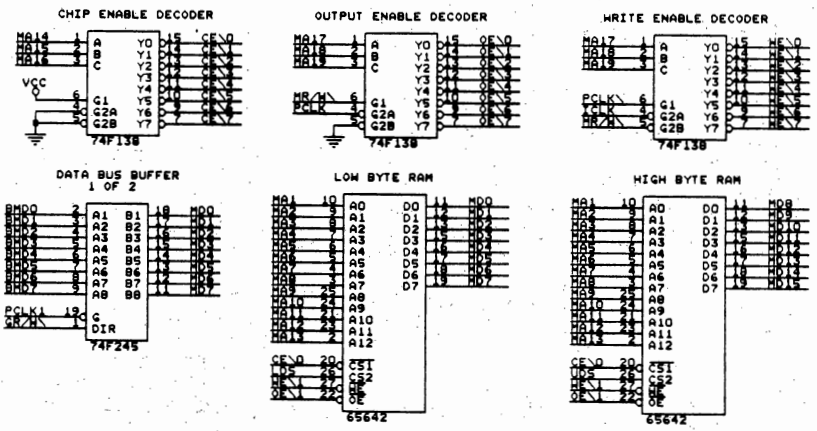
HARRIS RTX2000

INTERFACING TO RAMS: BUFFERED SYSTEM



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PARAMETER	10MHz	8MHz
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TAV: PCLK HIGH TO ADDRESS VALID	53ns	56ns
TDD: DECODE DELAY TIME	8ns	8ns
TBD: BUFFER DELAY TIME	7ns	7ns
TRDS: READ DATA VALID TO PCLK HIGH	12ns	12ns
TAA: MEMORY ADDRESS ACCESS TIME	20ns	42ns

NOTE:
ADDRESS MAY BE BUFFERED ONE LEVEL WITHOUT A SPEED PENALTY.
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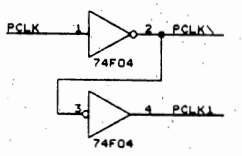
PCLK DELAY CIRCUIT



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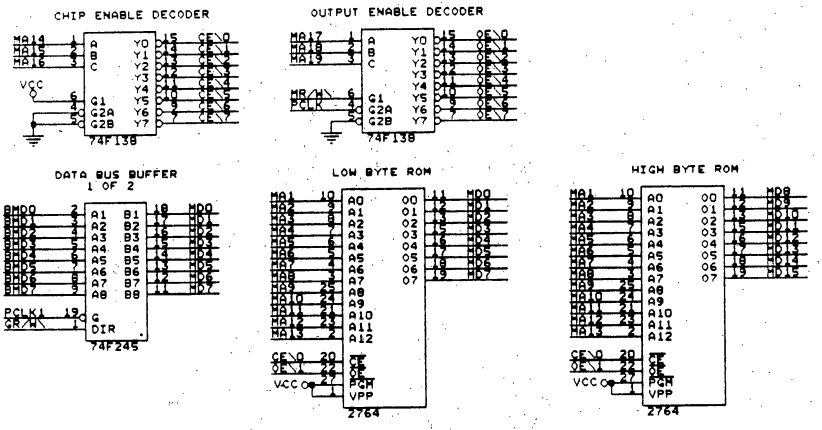
INTERFACING TO ROMS: BUFFERED SYSTEM



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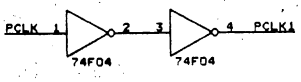

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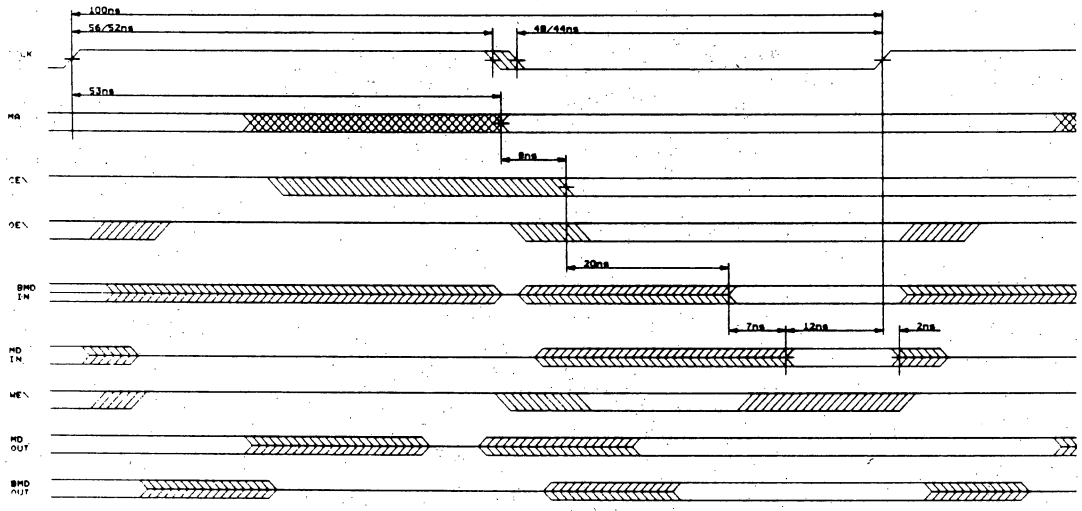
BUFFERED SYSTEM: 10MHz TIMING



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HARRIS RTX2000 ASIC BUS INTERFACE

OUTPUT PORT STROBED WITH GIO\ TIMING NOT CRITICAL

INPUT PORT TIMING CRITICAL STROBED EVERY READ CYCLE ON 74F540 OR 74AC540

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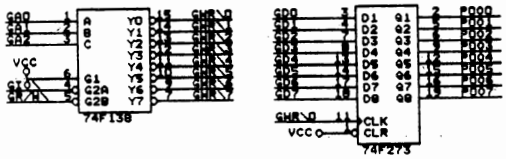
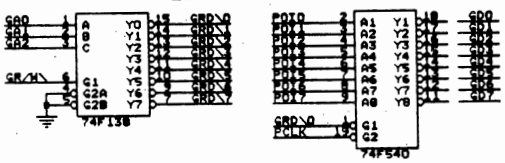
TYPICAL ASIC BUS INTERFACES

OUTPUT PORT



OUTPUT PORT DECODING IS GATED WITH GIO# TO ASSURE THAT OUTPUT LATCHES ARE ONLY STROBED AT CORRECT TIME.

INPUT PORT



INPUT PORT DECODING IS GATED WITH PCLK TO ALLOW MAXIMUM DATA SET UP TIME.

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The RTXDS Development System

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Overview

- The environment in which the Harris RTX2000 will be used is real-time embedded process control.
- The requirements for these systems as compared to conventional computer systems are unique:
- Custom designed hardware and unique I/O devices and interfaces.
- Interrupt driven, real-time and time critical applications.
- ROM based code and limited availability of RAM and ROM storage.

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Development Systems

- Embedded (or target) systems are generally inappropriate environments for the development of applications software.
- The target system most often lacks support for program development and testing:
  - no auxilary storage (disk),
  - no interface to a human operator (CRT/keyboard),
  - limited main storage (RAM),
- Lack of mature software support and development tools.

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Testing and Fault Isolation

- Excessive cost, in both dollars and in elapsed time, associated with the implementation of software has become of overriding concern in the design and development of computer systems.
- The software development phase most often underestimated, leading to cost and time overruns, is that of software testing and fault isolation.
- These problems are compounded in the testing of complex real-time embedded systems.

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Testing of Embedded Systems

- Development and testing of sophisticated embedded systems is often exceptionally costly and time consuming.
- Both the hardware as well as the software in such systems may be unique and under development. The system is being integrated as testing is conducted. As a result, faults are difficult to isolate.
- The demands of a real-time, interrupt driven systems, often with multi-tasking, may introduce race conditions that can be exceptionally difficult to reproduce and to debug.

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Testing of Embedded Systems

- The programmer or operator has little visibility into the system under test. Unlike more conventional computer systems, the responses of an embedded system often reflect second or third level effects that may be near useless in isolating programming errors.
- There are few peripheral devices on an embedded system that are useful in testing. There is no operator interface (CRT/keyboard) and limited internal storage.
- A digital analyzer is a useful tool but is sometimes awkward because of the microscopic level of detail provided.
- Lastly, there is no on-board software to facilitate testing of the programs.

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RTXDS

A Development Environment for Embedded Systems

Goals

The system must provide a FORTH interactive support environment.

The tools should be integrated to form a seamless development environment.

The programmer should be able to use symbolic references.

The target processor must be able to operate at full speed.

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RTXDS

The Host

- To build applications software in a productive and cost effective manner, we have chosen to implement much of the software support environment on a host computer system.
- The approach is an accepted and effective means of implementing embedded computer systems.
- The host and target are connected through a serial interface.
- The approach allows a unique software design environment; one that is a reliable combination of hardware and software-and one that is rich in both hardware facilities and in software support tools.

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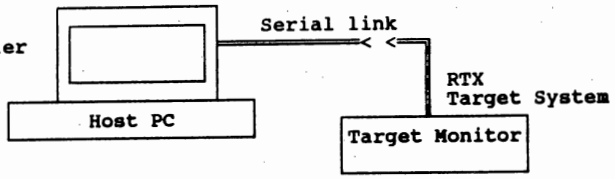
RTXDS Development Environment

RTXDS
Editor
TForth Cross-compiler
Disassembler
File Interface



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The Host

- We selected as a host the IBM (or compatible) PC with a full complement of facilities:

  Extensive internal storage,

  High volume external (disk) storage,

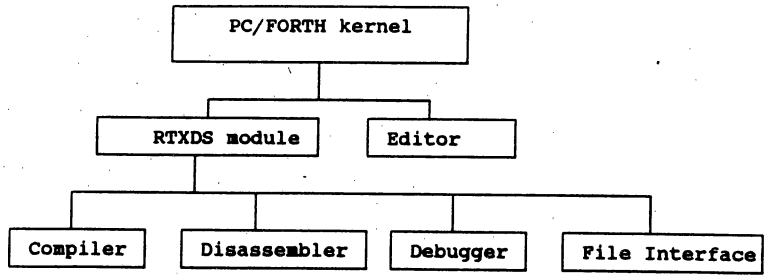
  Convenient human interface (CRT/keyboard),

  A sophisticated software build environment and mature support tools (LMI's PC/FORTH).

The Target

- The target system can be any board containing the Harris RTX 2000 processor along with minimal support hardware

RTXDS Structure



Development Tools

- In the RTXDS development environment, Harris provides a complete set of programming support tools to aid the programer.

TFORTH

The TFORTH cross compiler provides the software development engineer with a system to conveniently handle source programs and to generate ROMable object code for the processor.

Disassembler

The Disassembler is a software debug tool that converts binary object code into a sequence of the corresponding FORTH code.

File Interface

This set of modules provide the programmer with convenient access to disk files.

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Host/Target Serial Link

- A direct serial link from the host to the target facilities the software build process.
- The link provides a means of transferring object code from the host to the target to facilitate rapid prototyping of applications software.
- It also allows us to link the two subsystems in such a way that we not only provide the design engineer with an effective means for building source programs and generating target code, but in addition the link supports a powerful testing and fault isolation capability.

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RTXDS

Visibility and Control

- A major function of RTXDS is to provide a programmer/operator with visibility into a control of the system under test. The system provides a powerful set of utilities to support the application developer in debugging software.
- The debug facilities are designed and implemented using the host and target subsystems as an integrated software development facility -taking advantage of the capabilities of each subsystem in the design.

RTXDS

TFORTH Emulator

- The TFORTH cross compiler is as close as possible to a FORTH-83 system.
- The TFORTH Emulator provides a method of testing application source code with PC/FORTH on the host PC.
- The facility is useful for preliminary testing of an application.
- The emulator models the behavior of the RTX registers and the ASIC bus.

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RTXDS

- The system provides highly interactive control to the programmer testing software on the target subsystem.
- The programmer has the capability to temporarily stop the execution of programs in a unit test, and to examine and change the status of the target system.
- Programmer control is at the console of the host. The programmer is able to selectively trace the actions of programs executing on the target, to examine and to change processor registers and storage on the target subsystem.
- References to the variables and definitions within the target are symbolic. A dictionary is maintained in the host to map the symbols to the target addresses.

CONSOLE COMMANDS

```
>@   >C@

>!   >C!

>.S  >MOVE   >CMOVE

>DROP   >DUMP   >EXECUTE

>FILL  >.  >U.

>.REG   >.RR   >PUSH  >POP

>SET.BREAK   >CLR.BREAK

>DOWNLOAD   >UPLOAD

>G@  >G!  >GO

>LOAD
>:
```


RTXDS

VISIBILITY INTO THE TARGET

- DISPLAY FACILITIES THROUGH THE HOST ALLOW THE PROGRAMMER TO VIEW THE PROGRESS OF EXECUTION OF A PROGRAM UNDER TEST ON THE TARGET SUBSYSTEM.

- THESE FEATURES ARE INCORPORATED INTO THE TFORTH CROSS-COMPILER AS STANDARD FORTH FUNCTIONS.

- THE FEATURES ARE IMPLEMENTED SUCH THAT THESE DEBUG UTILITIES GENERATE NEITHER EXECUTION OVERHEAD NOR STORAGE REQUIREMENTS IN THE FINAL TARGET SYSTEM.

RTXDS

TFORTH Display Utilities

." EMIT

CR .

.S .REG

DUMP

Memory Reference Trace

>RANGE

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RTXDS

Breakpoint Facility

- We assume that in a test environment, that code as well as data will reside on the target subsystem in RAM.
- We include a capability to allow the programmer to insert a breakpoint into the code being tested.
- When a breakpoint is encountered during program execution, a transfer to the monitor is initiated automatically that allows the operator to gain control at the host console.
- The operator has the option to:

  Examine the target system status,

  Resume execution, or

  Cancel the breakpoint.

RTXDS

SUMMARY

- RTXDS PROVIDES THE PROGRAMMER WITH AN INTEGRATED FORTH ENVIRONMENT.
- IT IS SPECIFICALLY DESIGNED TO SUPPORT THE DEVELOPMENT OF REAL-TIME EMBEDDED SYSTEMS.
- OUR EXPERIENCE INDICATES THAT RTXDS OFFERS A FLEXIBLE AND PRODUCTIVE ENVIRONMENT FOR THE PROGRAMMER.

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HARRIS RTX SEMINAR

REAL TIME EXPRESS DEVELOPMENT BOARD

(RTXDB)

TIM DWYER
LEAD ENGINEER
HARDWARE SUPPORT DEVELOPMENT

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OVERVIEW

- o FEATURES
- o BLOCK DIAGRAM
- o MEMORY MAP
- o I/O PORTS
- o SERIAL PORT
- o PROTOTYPE AREAS
- o BOARD OPERATION

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FEATURES

- o BASED ON THE HARRIS RTX2000 PROCESSOR
- o FLEXIBLE AND EXPANDABLE
- o 16K BY 16 ZERO WAIT STATE STATIC RAM
- o 8K BY 16 SYSTEM PROM
- o UP TO 8K BY 16 USER PROM
- o 16-BIT INPUT AND OUTPUT PORTS
- o HIGH SPEED SERIAL PORT
- o PROTOTYPE AREAS

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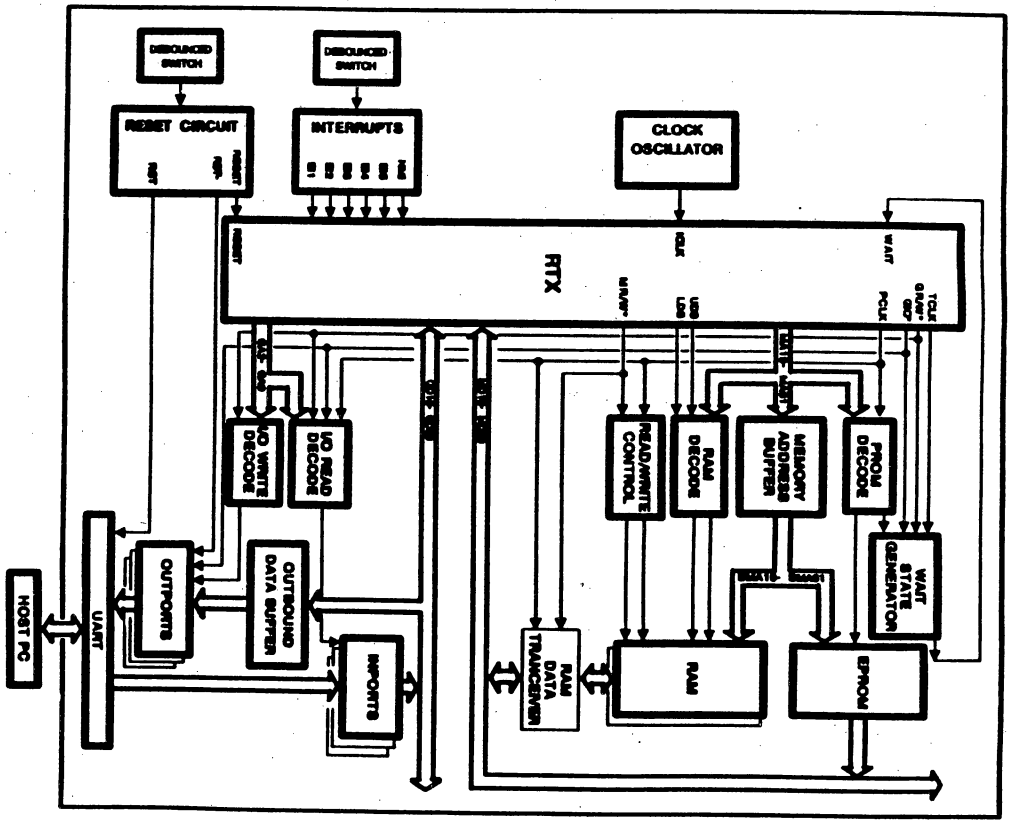

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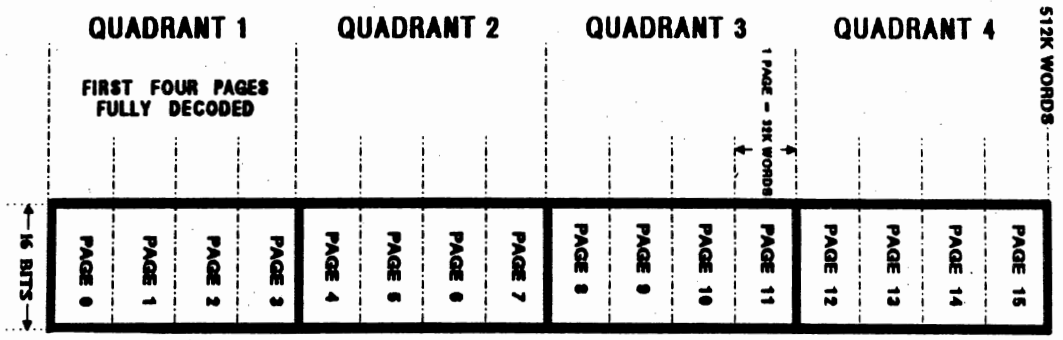
Memory Map



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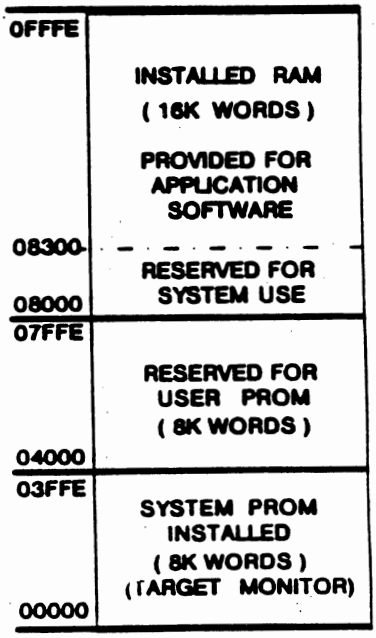
Memory Map, Page Zero



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I/O Ports

- Three 16 bit Output Ports (Latched)
- Three 16 bit Input Ports (Sampled)

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Serial Port

- Standard Baudrates up thru 19,200 Baud
- Status LEDs for data and handshake signals
- Header allows connector pinout to be changed

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Prototype Areas

- Allows RTXDB to be used as foundation for users prototype
- Allows expansion of RTXDB
- 20% of total board area
- Memory Area
  - Header with Memory Address, Data, and control signals
  - Up to four 28-Pin devices
- ASIC Bus Area
  - Header with G Address, Data and control signals
  - 24 by 28 array of plated holes For Pin Grid Array and other package types
  - Dual Inline Package (DIP) area For standard logic in DIPs

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Board Operation

- Green LED
  - Power On, Fuse intact
- Reset Switch
  - RTX2000, 82C50A, Parallel Output Ports
- Red LED
  - Blinking - After reset, RTXDB waiting for HOST to establish communication
  - On - RTXDB waiting for a command from the HOST
  - Off - RTXDB is executing instructions
- RS232 Connector
- Power connector

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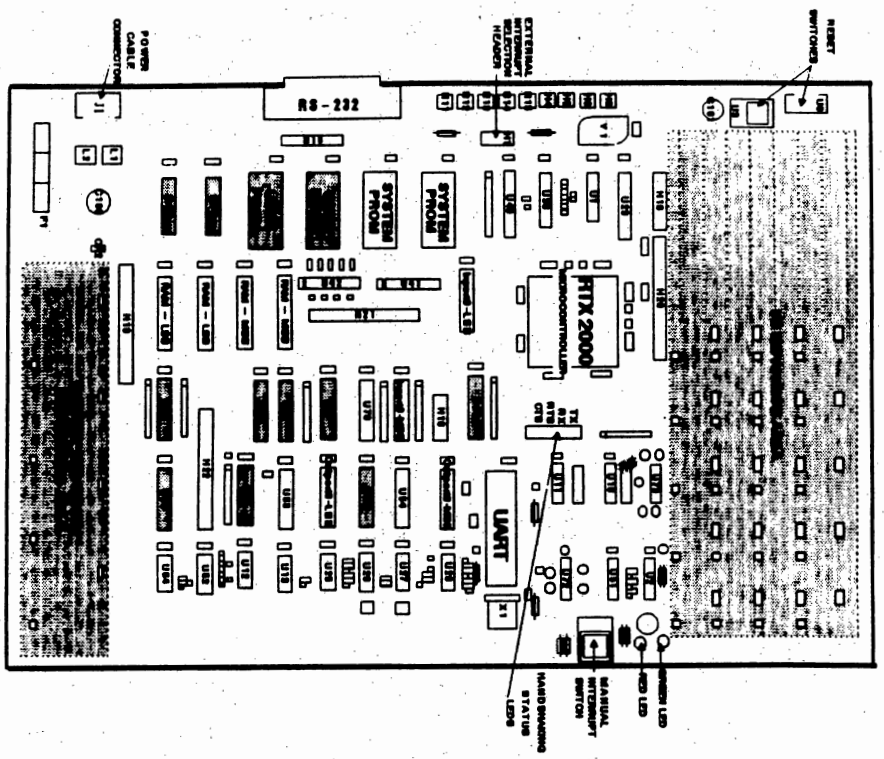

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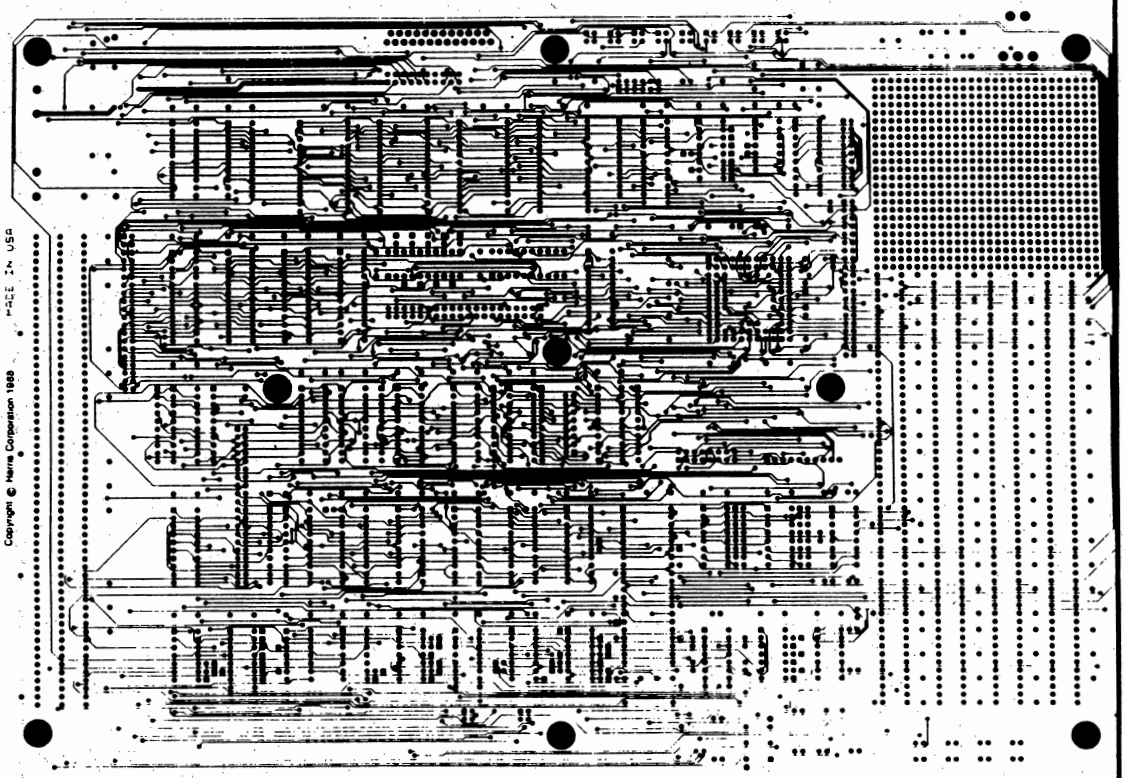

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TFORTH COMPILER

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TFORTH COMPILER

- FORTH-83 COMPATIBLE
- CROSS-COMPILES TO RTX MACHINE CODE
- OPTIMIZES FOR RTX ARCHITECTURE
- DESIGNED TO SUPPORT EMBEDDED CONTROL SYSTEMS
  - HEADERLESS CODE
  - DEBUGGING SUPPORT

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TForth Features

- Directives control compiler environment
- Compiles in separate blocks to support interrupts, vector tables, etc.
- Provisions for generating custom RTX instructions

  E842 UCODE @2+ => DUP @ SWAP 2+
- Can be used interactively from Host monitor

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TForth Memory Structure

- Compiles code into PC memory segment
- Maintains headers in separate Target Dictionary

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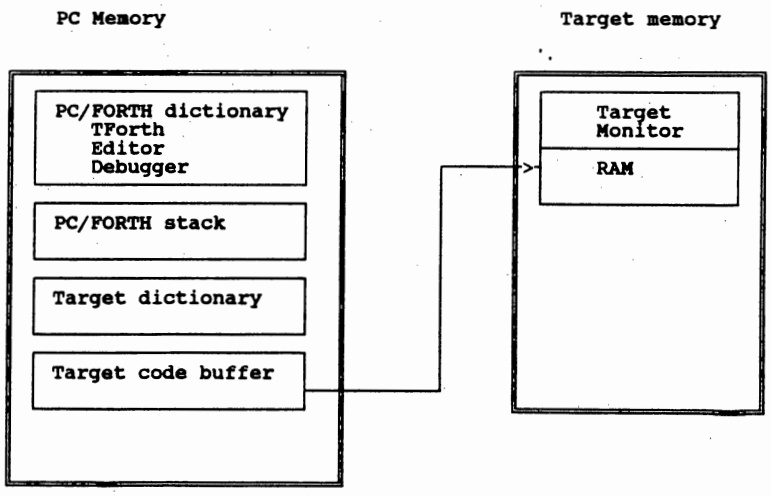
TForth Memory Map



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Compiler Directives

- All directives have defaults, some configurable
- Compiler invocation

  START-TFORTH - turns compiler on
  END-TFORTH - turns compiler off

- Memory configuration

  RAM-ONLY - all RAM
  RAM/ROM - separate memory spaces

- Memory addressing

  ROMORG - set code address
  RAMORG - set data address

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TForth Example

```
\ TForth Example 1
\ Calculates  2a + b - c
START-TFORTH
HEX 0000 ROMORG

: WORD1  ( a b c -- res )
  -  SWAP  DUP + + ;
: WORD2  2 3 4 WORD1 ;
END-TFORTH
```


Disassembler

- Decompiles RTX code to Forth primitives
- Useful for instruction sequencing and timing

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DISASSEMBLER INVOCATION

- 0 ADDR COUNT DASM
- 0 ADDR DASM; DISASSEMBLES ONE WORD
- 0 FULL DASM DISASSEMBLES ALL COMPILED CODE

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DISASSEMBLER EXAMPLE

```
Harris Semiconductor RTXDS Disassembler  V1.0                    Page  1
06/10/88     07:38     class.scr

Address Opcode  Operations

0000    : WORD1
        AC40     -
0002    AE80     SWAP
0004    A0C0     DUP
0006    A840      +
0008    A860      +  ;
000A    : WORD2
        BE42     LIT 02
000C    BE43     LIT 03
000E    BE44     LIT 04
0010    0000     WORD1                      Call 0000   '..'
0012    A020        ;
```


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RTX Extensions

- Registers and peripherals
  - IBC@ - reads Interrupt Base/Control Register
  - TC1! - writes value to Timer/counter 1
- Interrupts
  - directives for generating vector tables
  - SOFTINT - software interrupt
- ASIC Bus
  - G G@ - reads data from port G
  - N G G! - writes data to port G

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Optimization

- Combines subroutine return with last word of defintion
- Combines ALU and shift operations with previous instruction

  3 +
- Combines stack operations

  SWAP DROP => NIP

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Optimization Example

```
\ Optimization example

START-TFORTH
HEX 0000 ROMORG

: WORD3   2 SWAP -  SWAP DROP DUP ;

: WORD4   18 G@ + ;


END-TFORTH
```

```
0000    : WORD3
        BCC2    LIT 02  SWAP -
0002    A0A0    SWAP DROP DUP   ;

0004    : WORD4
        B8B8    18 G@   + ;
```


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Debug Support

- Terminal I/O supported through target monitor

  ." EMIT KEY

- Conditional compilation

  SWAP {{ ." Executing READ-DATA. Stack: " .S }} 2*

- Memory access trace

  All memory references (@ ! C@ C!) are routed through the monitor

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File Interface

- WRITE-HEX filename
  Generates Intel Hex file
- WRITE-IMAGE filename
  Generates object file
- READ-IMAGE filename
  Reads image file
- READ-HEX filename
  Reads hex file
- FTYPE filename
  Similar to DOS TYPE command
- FDUMP filename
  HEX/ASCII dump

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Exercise

Object: Write a program which flashes "SOS" in Morse code on the LED on the front of the box.

Hints: The LED is turned on by writing 8000H to port 18H:

```
8000 18 G!
```

The LED is turned off by writing 0000H to the port.

SOS is 3 short flashes, followed by 3 long flashes, followed by 3 short flashes

Gentlemen, start your code at 8300H:

```
8300 ROMORG
```

If you have time

Write the following so that they may be compiled with either PC/FORTH or TForth.

1. Write a program to calculate the Nth Fibonacci number Fn:
   F0 = 0 F1 = 1
   Fk = Fk-1 + Fk-2 for k > 1

2. Write a program to calculate N! for any N, 0 <= N <= 8

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