BINAR™ Evaluation Board Reference

Preliminary - Version 0.0

March 1, 1990

BINAR EVALUATION BOARD

The BINAR evaluation board has been designed to provide an evaluation platform for the BINAR core processor. In addition to the BINAR processor, the board contains hardware for an IBM PC bus interface, memory support, and a parallel port. Additional features include a small prototyping area and three sets of header pins that provide quick access to the board's bus signals.

The PC bus interface is a standard 8-bit interface that allows the evaluation board to use the PC as an I/O terminal. The evaluation board is mapped into the PC I/O space using a base address of 300 Hex. (If this particular base address is already being used, the user can change to another base address by reprogramming PAL chip U11.) The host PC I/O addresses used to interface to the evaluation board are as follows:

READ OPERATIONS:

300 Hex - Read byte 0 from the BINAR Evaluation board to the PC and reset BOARD_READY signal.

301 Hex - Read byte 1 from the BINAR Evaluation board to the PC.

302 Hex - Read byte 2 from the BINAR Evaluation board to the PC.

303 Hex - Read byte 3 from the BINAR Evaluation board to the PC.

304 Hex - Cycle OSC to perform a read-from-board operation.

305 Hex - Read status from BINAR Evaluation board, where:
bit 0 = Master mode
bit 1 = Test mode
bit 2 = DMA read to PC mode
bit 3 = DMA write from PC mode
bit 4 = Board is ready for data (BOARD_READY)

WRITE OPERATIONS:

300 Hex - Write byte 0 to BINAR Evaluation board from PC and set HOST_READY signal.

301 Hex - Write byte 1 to BINAR Evaluation board from PC.

302 Hex - Write byte 2 to BINAR Evaluation board from PC.

303 Hex - Write byte 3 to BINAR Evaluation board from PC.

304 Hex - Cycle OSC to perform a write-to-board operation.

305 Hex - Write status to BINAR Evaluation board, where:
bit 0 = Master mode
bit 1 = Test mode
bit 2 = DMA read to PC mode
bit 3 = DMA write from PC mode.

307 Hex - Resets board by clearing HOST_READY, BOARD_READY, Master mode, Test mode, DMA modes, and asserts RESET pin on BINAR. Same operation is performed when the PC RESET line is active.

The BINAR Evaluation Board I/O addresses for interfacing to the host PC are as follows. Note that only bits RAD2 and RAD3 are actually decoded by the board.

READ OPERATIONS:

007FFFF0 Hex - Performs a 32-bit transfer from the board holding registers to BINAR and resets the HOST_READY signal.

007FFFF4 Hex - Returns the status of the HOST_READY signal in bit 0 of the result, other bits returned are undefined.

007FFFF8 Hex - Transfers 8 bits of data from the Parallel I/O Port Input Register.

007FFFFC Hex - RESERVED, must be left unused.

WRITE OPERATIONS:

007FFFF0 Hex - Performs a 32-bit transfer to the board holding registers from BINAR and sets the BOARD_READY signal.

007FFFF8 Hex - Transfers 8 bits of data to the Parallel I/O Port Output Register.

007FFFFC Hex - RESERVED, must be left unused.

The BINAR Evaluation board provides support for 128K x 32 bits of static RAM memory (i.e. 512K bytes). This memory is divided into four banks of 32K x 32 bits. Each bank consists of four 32K x 8 static memory chips. A minimum of one bank of memory must be populated for evaluation purposes. If fewer than four banks are to be populated, the lowest numbered memory banks should be used first. For example, if only two banks are going to be populated, they should be BANK0 and BANK1. Memory bank : IC Sockets correspondence is as follows:

BANK0 - U32, U33, U34, & U35
BANK1 - U28, U29, U30, & U31
BANK2 - U24, U25, U26, & U27
BANK3 - U20, U21, U22, & U23

In addition to the requirement for populating correct sockets, each bank of memory has a BANK#\ select signal which must be enabled (# denotes the corresponding memory bank number). The BANK#\ signals are the output of a 3 to 8 decoder chip. The inputs to the decoder come from a 6 X 2 header. Jumpers must be placed on the header to selectively enable the appropriate BANK#\ signals. This is required to map the high end of the BINAR address range (used for booting and interrupt vectors) into the installed memory chips.

If only one bank of memory has been installed, jumper clips should be placed on headers: JP2, JP4, and JP6. This jumper configuration will enable the BANK0\ select signal. Note that with this configuration, any attempted memory write operation to an address above the 128K byte boundary will result in a write operation being performed on BANK0, with possible corruption of data.

If two banks of memory are installed, jumper clips should be placed on headers JP1, JP4, and JP6. Either the BANK0\ or

BANK1\ select signal will be active during a memory operation. When this configuration is set, it is important to note that any attempt to perform a memory write operation above the 256K byte boundary will result in a write operation being performed on the lower two banks of memory, with possible corruption of data.

If four banks of memory are installed, jumper clips should be placed on headers JP1, JP3, and JP6. Either the BANK0\, BANK1\, BANK2\, or BANK3\ select signal will be active during a memory operation. When this configuration is set, it is important to note that any attempt to perform a memory write operation above the 512K byte boundary will result in a write operation being performed on the lower two banks of memory, with possible corruption of data.

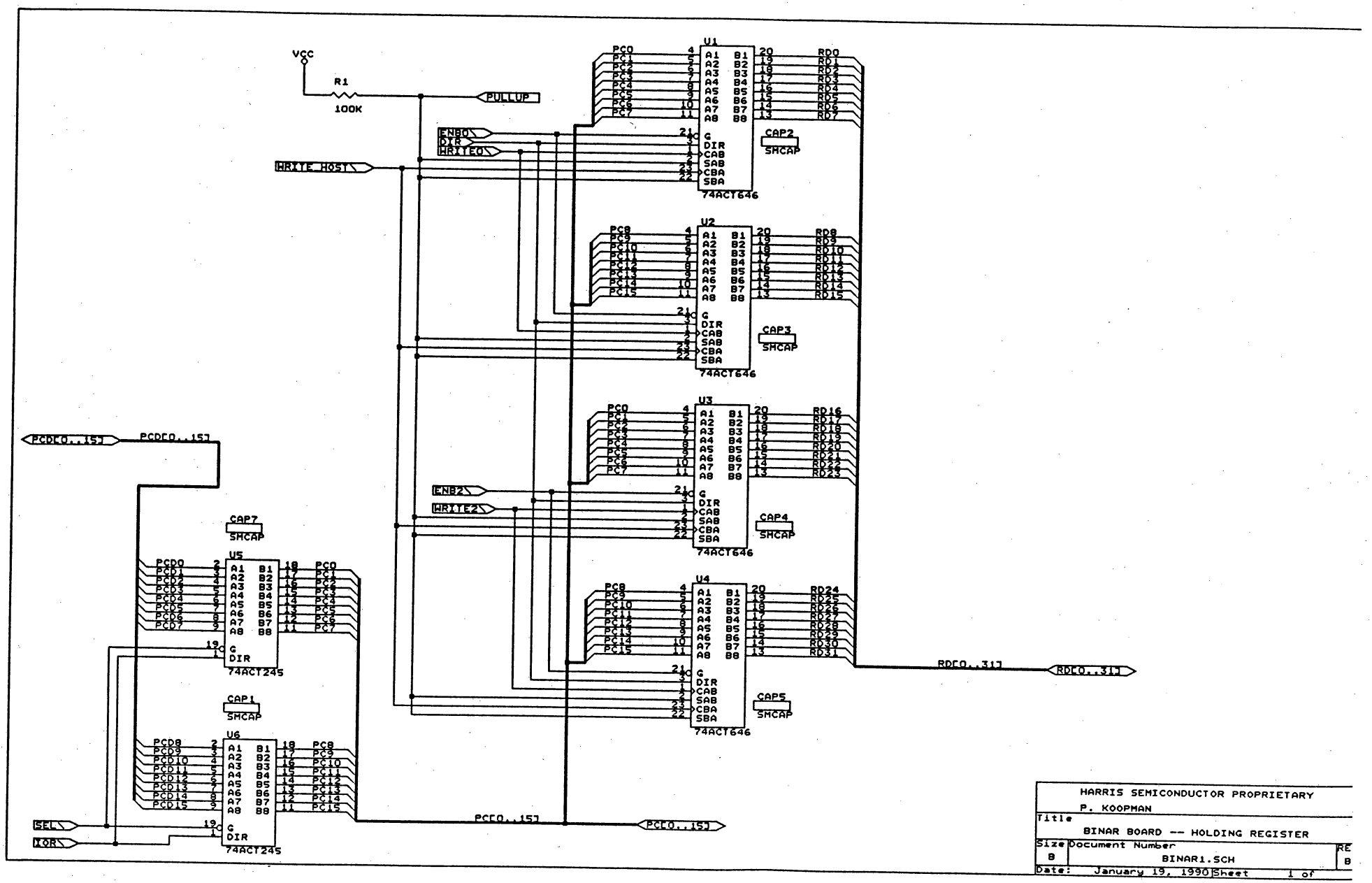
The use of three banks of memory is not recommended.

PAL EQUATIONS

```
module BINAR
title 'PC plug-in board for BINAR
converted from PALASM files by phil koopman
krl 10/30/89'

U11_DEC_SEL,U14_STATE device 'P16V8R';
U16_KITCHEN,U40_RD_DEC,U15_ASIC_DEC device 'P16V8C';
U13_WR_DEC device 'P16V8C';

!ALE,PCAD3,PCAD4,PCAD5,PCAD6 pin in U11_DEC_SEL 1,2,3,4,5;
PCAD7,PCAD8,PCAD9,AEN,OE     pin in U11_DEC_SEL 6,7,8,9,11;
!WRITE4,!SLOWEST4            pin in U11_DEC_SEL 12,13;
!DECODED,!SEL                pin in U11_DEC_SEL 17,18;
!SLOW4                       pin in U11_DEC_SEL 19;

PCAD0,PCAD1,PCAD2,IOR,!SEL   pin in U40_RD_DEC 1,2,3,4,5;
!READ_HOST,!WRITE4,!READ0    pin in U40_RD_DEC 6,7,12;
!READ4,!READ5,!ENB0          pin in U40_RD_DEC 13,14,15;
!ENB1,!ENB2,!ENB3,DIR        pin in U40_RD_DEC 16,17,18,19;

PCAD0,PCAD1,PCAD2,IOW,!SEL   pin in U13_WR_DEC 1,2,3,4,5;
PC_RESET,DMA_READ            pin in U13_WR_DEC 6,7;
DMA_WRITE,BOARD_READY        pin in U13_WR_DEC 8,9;
HOST_READY,!WRITE0,!WRITE1   pin in U13_WR_DEC 11,12,13;
!WRITE2,!WRITE3,!WRITE4      pin in U13_WR_DEC 14,15,16;
!WRITE5,!XRES,!NEED_DMA_XFER pin in U13_WR_DEC 17,18,19;

STATE_CLK,PC0,PC1,PC2,PC3    pin in U14_STATE 1,2,3,4,5;
!RESET,!DMA_ACK,T_C,!WRITE5  pin in U14_STATE 6,7,8,9;
!READ5,MASTER,!TEST,STATE0   pin in U14_STATE 11,12,13,14;
STATE1,STATE2,STATE3         pin in U14_STATE 15,16,17;
DMA_READ,DMA_WRITE           pin in U14_STATE  18,19;

RAD2,RAD3,!ASIC,!OE,!WR0     pin in U15_ASIC_DEC 1,2,3,4,5;
!READ0,!WRITE0,!DMA_ACK,IOR  pin in U15_ASIC_DEC 6,7,8,9;
IOW,!READ_HOST,!WRITE_HOST   pin in U15_ASIC_DEC 11,12,13;
!READ_STATUS,!READ_I_O       pin in U15_ASIC_DEC 14,15;
!WRITE_I_O,!BOARD_TAKE,!READ4  pin in U15_ASIC_DEC 16,17,18;
!HOST_PUT                    pin in U15_ASIC_DEC 19;

IOR,IOW,!SEL                 pin in U16_KITCHEN 1,2,3;
DMA_READ,DMA_WRITE           pin in U16_KITCHEN 4,5;
!DMA_ACK,!XRES,T_C,!WRITE5   pin in U16_KITCHEN 6,7,8,9;
!CHIP_RESET,!XENB,STATE_CLK  pin in U16_KITCHEN 13,14,15;
!READ_STATUS,!RESET,!READ5   pin in U16_KITCHEN 16,17,18;
BOARD_READY,RD3,PC4          pin in U16_KITCHEN 11,12,19;
```

```
EQUATIONS in U11_DEC_SEL
" CLOCK FOR DECODED IS /ALE
" DECODED FOR $300,  Other addresses will change this
equation

DECODED :=  PCAD9 &  PCAD8 & !PCAD7 & !PCAD6 &
           !PCAD5 & !PCAD4 & !PCAD3;

SEL = DECODED & !AEN;

!SLOW4 = !WRITE4;
!SLOWEST4 = !SLOW4;


EQUATIONS  in U40_RD_DEC
READ0  = IOR & SEL & !PCAD2 & !PCAD1 & !PCAD0;
READ4  = IOR & SEL &  PCAD2 & !PCAD1 & !PCAD0;
READ5  = IOR & SEL &  PCAD2 & !PCAD1 &  PCAD0;

"   enbx = read_host # readx

ENB0 = READ_HOST #  WRITE4  #
                    IOR & SEL & !PCAD2 & !PCAD1 & !PCAD0;
ENB1 = READ_HOST #  WRITE4  #
                    IOR & SEL & !PCAD2 & !PCAD1 &  PCAD0;
ENB2 = READ_HOST #  WRITE4  #
                    IOR & SEL & !PCAD2 &  PCAD1 & !PCAD0;
ENB3 = READ_HOST #  WRITE4  #
                    IOR & SEL & !PCAD2 &  PCAD1 &  PCAD0;

"  dir true passes data from PC to CPU

!DIR =  IOR & SEL & !PCAD2;


EQUATIONS  in U13_WR_DEC
WRITE0 = IOW  & SEL & !PCAD2 & !PCAD1 & !PCAD0;
WRITE1 = IOW  & SEL & !PCAD2 & !PCAD1 &  PCAD0;
WRITE2 = IOW  & SEL & !PCAD2 &  PCAD1 & !PCAD0;
WRITE3 = IOW  & SEL & !PCAD2 &  PCAD1 &  PCAD0;
WRITE4 = IOW  & SEL &  PCAD2 & !PCAD1 & !PCAD0;
WRITE5 = IOW  & SEL &  PCAD2 & !PCAD1 &  PCAD0;

XRES = PC_RESET #  IOW & SEL &  PCAD2 &  PCAD1 &  PCAD0;

NEED_DMA_XFER =  DMA_WRITE & !HOST_READY  #
                              DMA_READ & BOARD_READY;

EQUATIONS in U14_STATE
```

```
!STATE0 := !PC0;
!STATE1 := !PC1;
!STATE2 := !PC2;
!STATE3 := !PC3;

!MASTER     = !STATE0;
TEST        =  STATE1;
!DMA_READ   = !STATE2;
!DMA_WRITE  = !STATE3;

EQUATIONS in U15_ASIC_DEC

READ_HOST    =    !RAD2 & !RAD3   & ASIC & OE;

WRITE_HOST   =    !RAD2 & !RAD3   & ASIC & WR0 # READ4;

READ_STATUS =     RAD2 & !RAD3   & ASIC & OE;

READ_I_O     =    !RAD2 &  RAD3   & ASIC & OE;

WRITE_I_O     =   !RAD2   & RAD3   & ASIC & WR0;

BOARD_TAKE =   IOR & DMA_ACK   #   READ0;

HOST_PUT    =   IOW & DMA_ACK   #   WRITE0;


EQUATIONS in U16_KITCHEN

XENB = SEL;

!STATE_CLK =   WRITE5;

RESET = !CHIP_RESET & !XRES;

CHIP_RESET = !RESET & !READ5;

PC4 = BOARD_READY;
    enable PC4 = READ5;

RD3 = BOARD_READY;
    enable RD3 = READ_STATUS;
end
```



HARRIS SEMICONDUCTOR PROPRIETARY

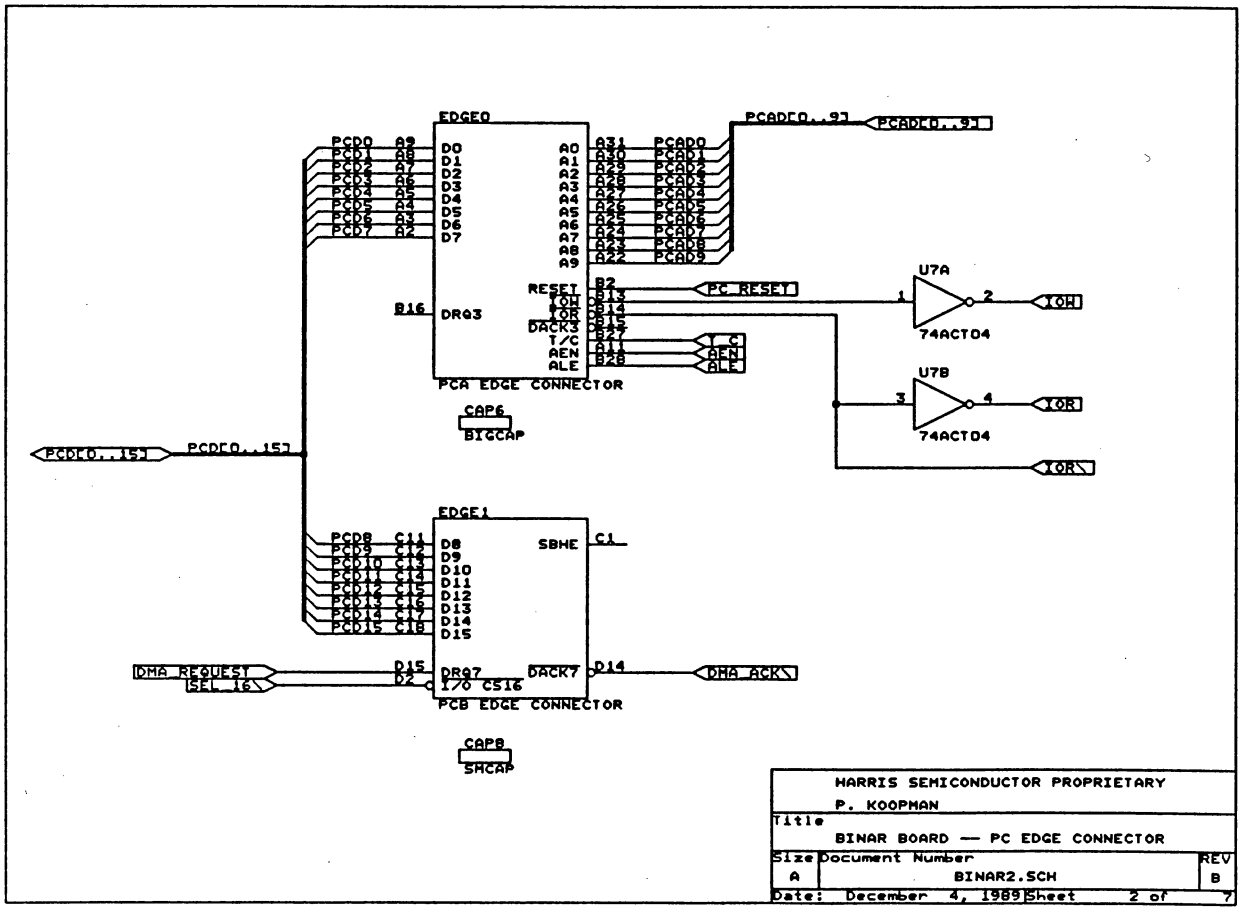
P. KOOPMAN

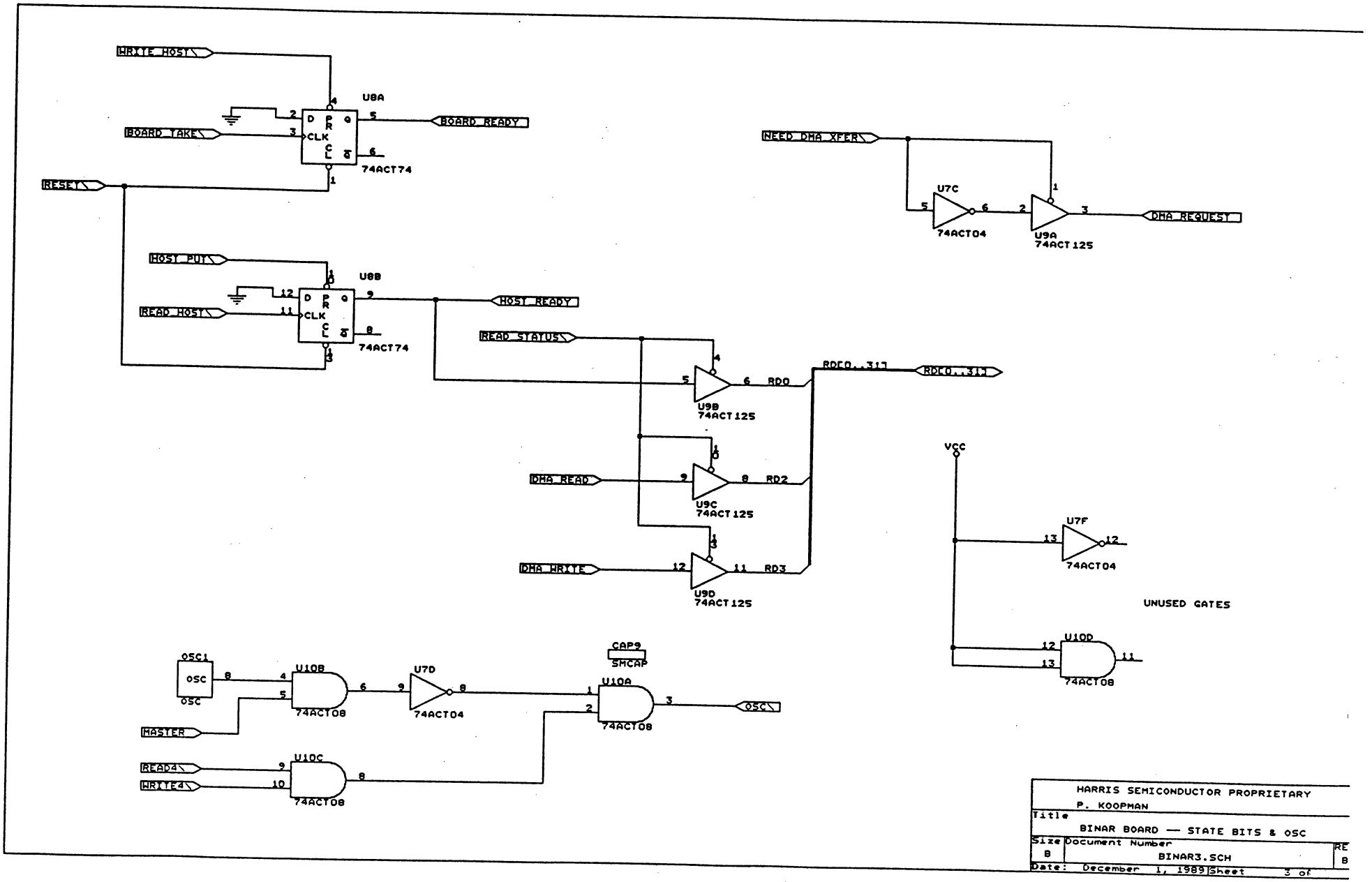
Title

BINAR BOARD -- HOLDING REGISTER

Size	Document Number	RE
B	BINAR1.SCH	B

Date: January 19, 1990 Sheet 1 of


EDGE0
PCD0
PCD1
PCD2
PCD3
PCD4
PCD5
PCD6
PCD7
D0
D1
D2
D3
D4
D5
D6
D7
B16
DRQ3
RESET
IOW
IOR
DACK3
T/C
AEN
ALE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
PCAD0
PCAD1
PCAD2
PCAD3
PCAD4
PCAD5
PCAD6
PCAD7
PCAD8
PCAD9
PCADR0..9]
PCADR0..9]
PC_RESET
T_C
AEN
ALE
PCA EDGE CONNECTOR
CAP6
BIGCAP
U7A
U7B
74ACT04
74ACT04
IOH
IOR
IOR\
PCDR0..15]
PCDR0..15]
EDGE1
PCD8
PCD9
PCD10
PCD11
PCD12
PCD13
PCD14
PCD15
D8
D9
D10
D11
D12
D13
D14
D15
SBHE
C1
DMA_REQUEST
SEL_16\
DRQ7
I/O CS16
DACK7
D14
DMA_ACK\
PCB EDGE CONNECTOR
CAP8
SMCAP
HARRIS SEMICONDUCTOR PROPRIETARY
P. KOOPMAN
Title
BINAR BOARD — PC EDGE CONNECTOR
Size
A
Document Number
BINAR2.SCH
REV
B
Date: December 4, 1989
Sheet 2 of 7



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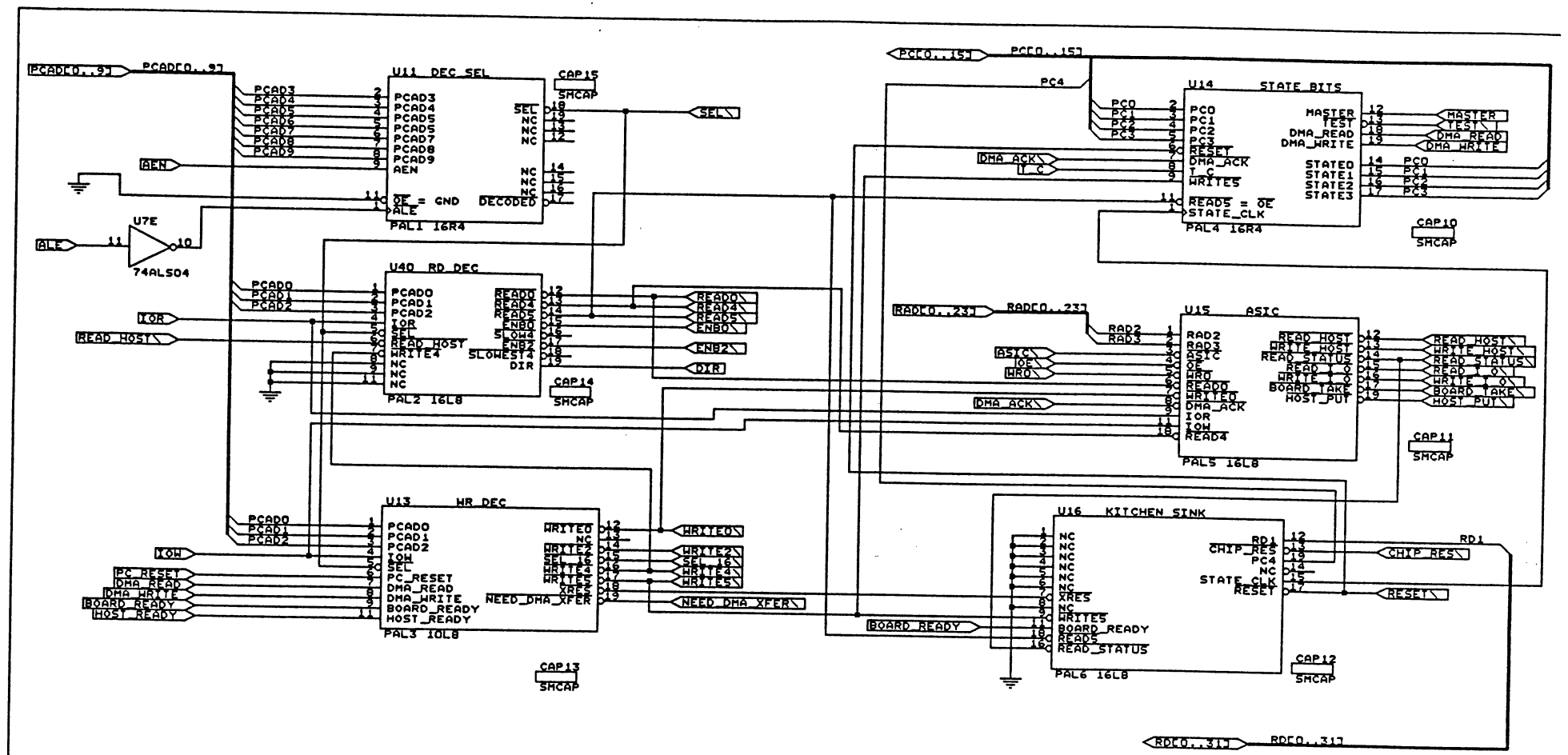
Title: BINAR BOARD — STATE BITS & OSC

Size	Document Number	RE
B	BINAR3.SCH	B

Date: December 1, 1989 Sheet 3 of



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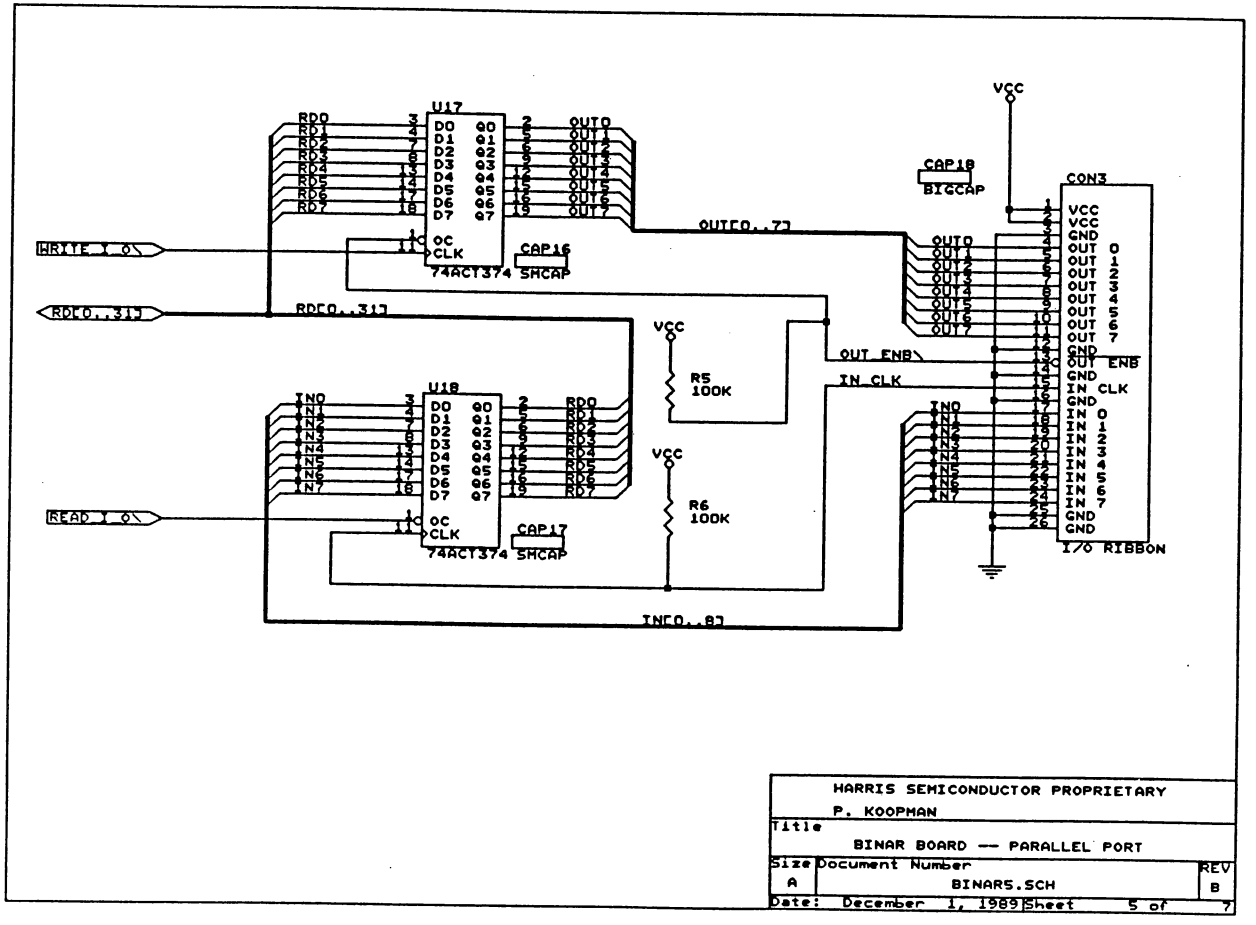
P. KOOPMAN

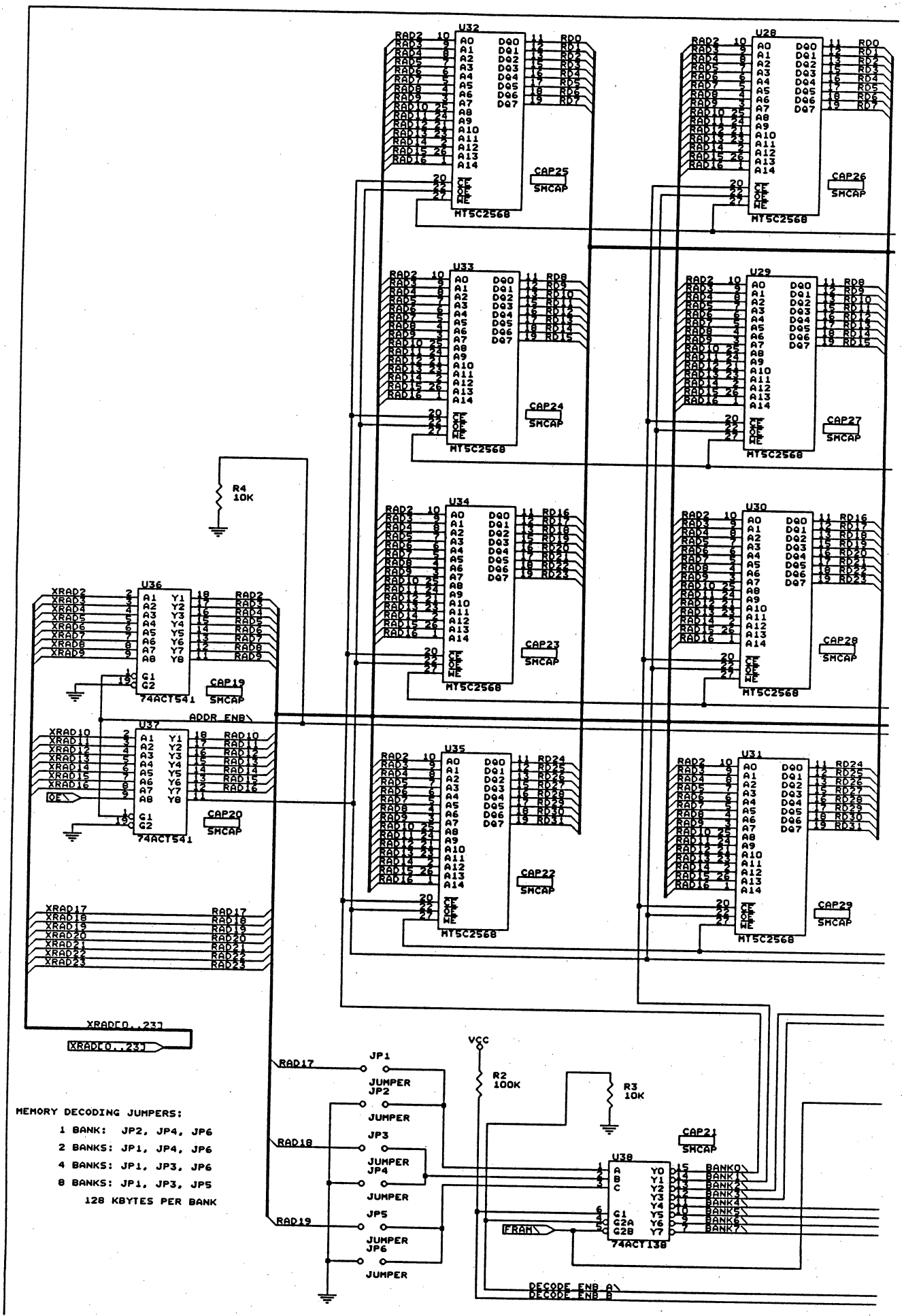
Title: BINAR BOARD -- PLDs

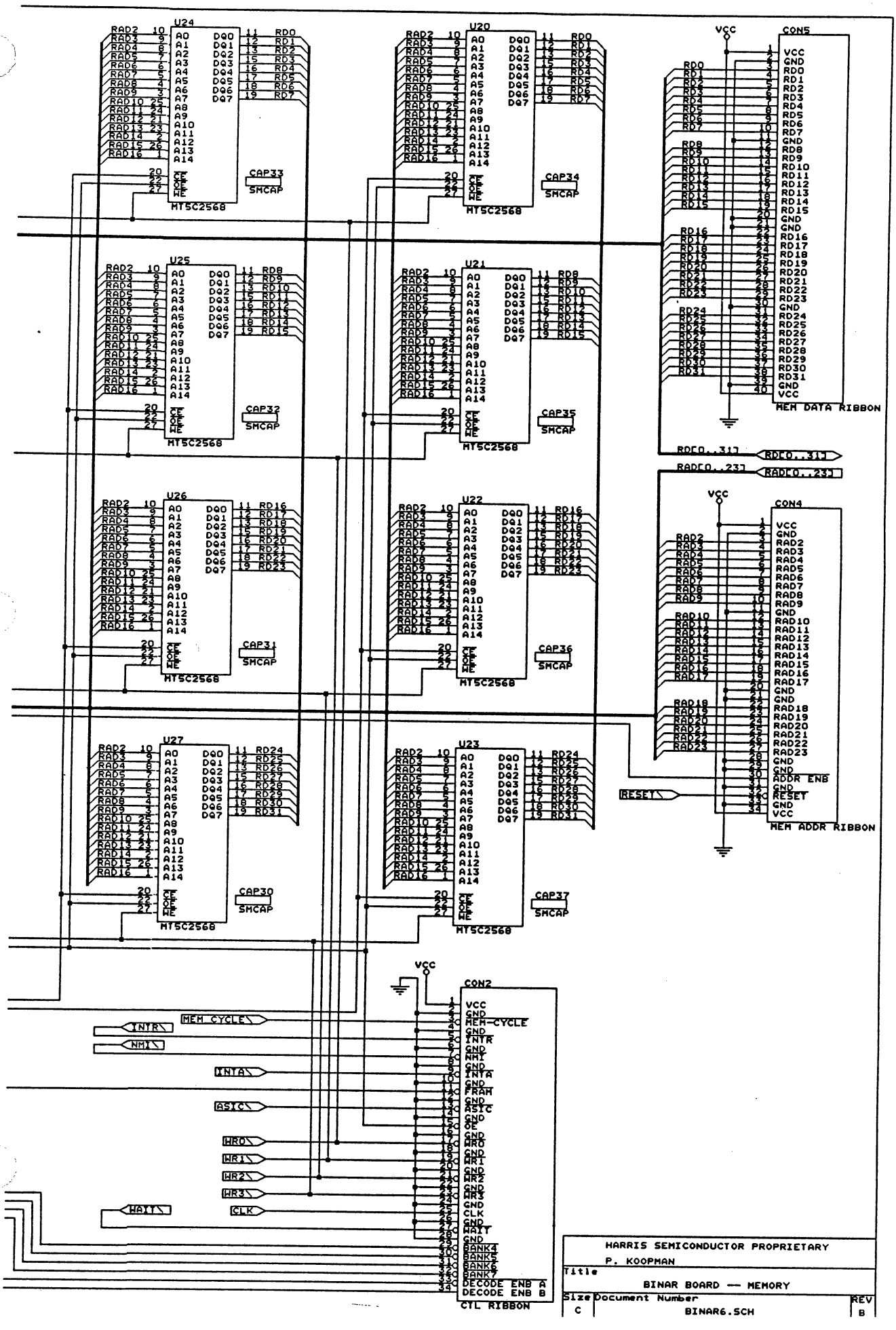
Size: B | Document Number: BINAR4.SCH | RE: B

Date: December 4, 1989 | Sheet 4 of



HARRIS SEMICONDUCTOR PROPRIETARY		
P. KOOPMAN		
Title: BINAR BOARD — PARALLEL PORT		
Size: A	Document Number: BINARS.SCH	REV: B
Date: December 1, 1989	Sheet 5 of 7	


U32
U28
U33
U29
U34
U30
U35
U31
MT5C2568
CAP25
CAP26
CAP24
CAP27
CAP23
CAP28
CAP22
CAP29
SMCAP
R4
10K
U36
U37
74ACT541
CAP19
CAP20
ADDR_ENB\
XRAD[0..23]
XRAD[0..23]
JP1
JP2
JP3
JP4
JP5
JP6
JUMPER
RAD17
RAD18
RAD19
VCC
R2
100K
R3
10K
CAP21
U38
74ACT138
FRAM\
DECODE_ENB_A\
DECODE_ENB_B\
MEMORY DECODING JUMPERS:
1 BANK: JP2, JP4, JP6
2 BANKS: JP1, JP4, JP6
4 BANKS: JP1, JP3, JP6
8 BANKS: JP1, JP3, JP5
128 KBYTES PER BANK



HARRIS SEMICONDUCTOR PROPRIETARY

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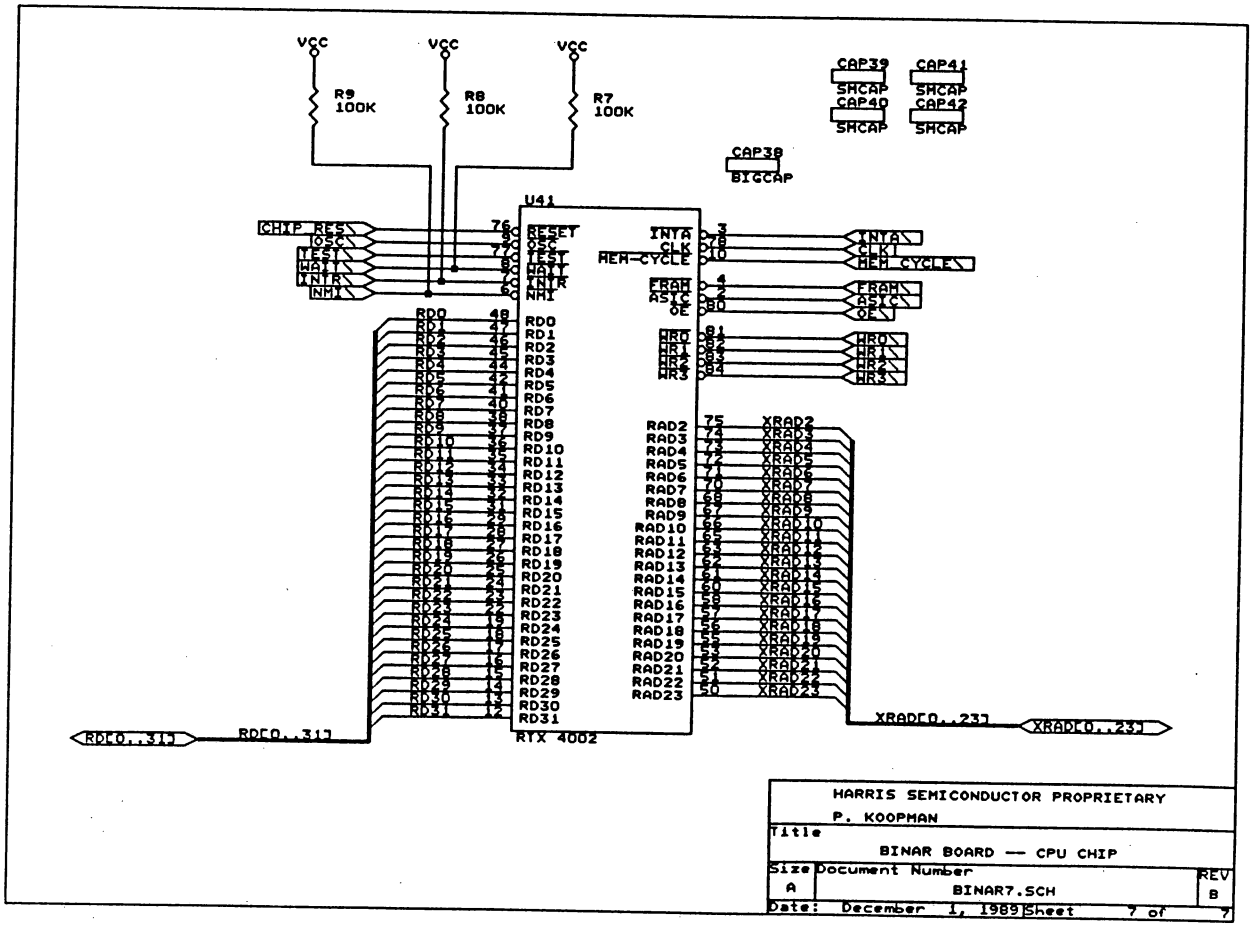
Title

BINAR BOARD — MEMORY

Size	Document Number	REV
C	BINAR6.SCH	B


VCC
VCC
VCC
R9
100K
R8
100K
R7
100K
CAP39
SHCAP
CAP41
SHCAP
CAP40
SHCAP
CAP42
SHCAP
CAP38
BIGCAP
U41
CHIP RES
OSC
TEST
WAIT
INTR
NMI
RESET
OSC
TEST
WAIT
INTR
NHI
INTA
CLK
MEM-CYCLE
FRAM
ASIC
OE
HR0
HR1
HR2
HR3
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
RD12
RD13
RD14
RD15
RD16
RD17
RD18
RD19
RD20
RD21
RD22
RD23
RD24
RD25
RD26
RD27
RD28
RD29
RD30
RD31
RAD2
RAD3
RAD4
RAD5
RAD6
RAD7
RAD8
RAD9
RAD10
RAD11
RAD12
RAD13
RAD14
RAD15
RAD16
RAD17
RAD18
RAD19
RAD20
RAD21
RAD22
RAD23
XRAD2
XRAD3
XRAD4
XRAD5
XRAD6
XRAD7
XRAD8
XRAD9
XRAD10
XRAD11
XRAD12
XRAD13
XRAD14
XRAD15
XRAD16
XRAD17
XRAD18
XRAD19
XRAD20
XRAD21
XRAD22
XRAD23
RTX 4002
RDFD[0..31]
RDFD[0..31]
XRADFD[0..23]
XRADFD[0..23]
HARRIS SEMICONDUCTOR PROPRIETARY
P. KOOPMAN
Title
BINAR BOARD — CPU CHIP
Size
A
Document Number
BINAR7.SCH
REV
B
Date: December 1, 1989
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