ECE 18-760      FALL 2001
VLSI CAD: Logic to Layout

FACULTY
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MEETING TIMES
Tuesday, Thursday 12:30 - 2:20pm, HH B131

CLASS WEB PAGE
http://www.ece.cmu.edu/~ee760

PRE-REQUISITES
Necessary Background
15-211, 15-212
18-240

Comments about Assumed Skills
Basic CS data structures and algorithms, programming in C language, UNIX
Basic digital design and verification, with combinational and sequential logic
Some exposure to VLSI ideas
18-321 or 18-322, or by permission

TEXTBOOKS
Also, extensive lecture notes will be provided.

INTENDED AUDIENCE
Graduate students and serious seniors interested in a broad exposure to the ideas behind the design of the algorithms inside VLSI CAD tools for logic and layout.

ASSIGNMENTS
Assignment Description % of Grade
6 Homeworks Analysis & design of algorithms and small programs that illustrate core CAD ideas 40%
3 Projects Programming assignments (JAVA/C++/UNIX) to build CAD tools 45%
3 Paper reviews Analysis of topics from current CAD literature 15%

WHAT 18-760 IS NOT
A circuits class. A design class where you mostly use other people’s CAD tools. Another class involving only mindless hacking (as opposed to thinking). Math-free, i.e., there’s some discrete math in this class, and some continuous math.

WHAT 18-760 IS
An applied algorithms class. A class where you get to look inside CAD tools and see what makes them work. A natural bridge between CE and CS applications and ideas. A class where you get to build (simplified chunks of) VLSI CAD tools. A good course for would-be CAD folks, or would-be VLSI designers, or folks just interested in nice algorithms that deal with 1s and 0s, graphs, time & waveforms, polygons.
TENTATIVE SYLLABUS (i.e., things may change...) | HW | Proj | Paper
---|---|---|---
WEEK 1 8/28 | Introduction to CAD flow of ICs; Advanced Boolean Algebra |  |  
| 8/30 | Advanced Boolean Algebra, cont. | hw1 |  
WEEK 2 9/4 | Advanced Boolean Algebra, cont. |  |  
| 9/6 | JAVA Language Review |  | Proj1  
WEEK 3 9/11 | Boolean Representation: BDDs |  |  
| 9/13 | Boolean Representation: BDDs, cont | hw2 | Pap1  
WEEK 4 9/20 | Formal Verification: Finite State Machine Equiv |  |  
WEEK 5 9/25 | Formal Verification: FSM Equivalence, continued | hw3 |  
| 9/27 | 2-Level Logic Synthesis: ESPRESSO |  |  
WEEK 6 10/2 | 2-Level Logic Synthesis: ESPRESSO, cont. |  |  
| 10/4 | Multilevel Logic Synthesis: Boolean Network Model |  | hw4  
WEEK 7 10/9 | Multilevel Logic Synthesis: Algebraic Division |  | Proj2  
| 10/11 | Project 2 Review |  | Pap2  
WEEK 8 10/16 | Multilevel Logic Synthesis: Rectangle Covering |  |  
| 10/18 | Multilevel Logic Synthesis: Rectangle Covering, cont | hw5 | Proj3  
WEEK 9 10/23 | Multilevel Logic Synthesis: Role of Don’t Cares |  | Pap3  
| 10/25 | Technology Mapping |  |  
WEEK 10 10/30 | Component Placement for ASICs |  |  
| 11/1 | Component Placement for ASICs, cont | hw6 |  
WEEK 11 11/6 | Component Placement for ASICs, cont |  | RAR away; guest lec  
| 11/8 | Component Routing for ASICs |  |  
WEEK 12 11/13 | Project 3 Review |  |  
| 11/14 | Component Routing for ASICs, cont |  |  
WEEK 13 11/20 | Static Timing Analysis. |  |  
| 11/22 | NO CLASS--THANKSGIVING BREAK |  |  
WEEK 14 11/27 | Static Timing Analysis, cont. |  | RAR away; guest lecs  
| 11/29 | Electrical Delay Analysis |  |  
WEEK 15 12/4 | Geometric Data Structures for Analysis & Verification |  |  
| 12/6 | Geometric Data Structures, cont. |  | RAR away; guest lec  
WEEK 16 12/11 | Geometric Data Structures, cont. |  |  

**Note:** Revised deadlines here

RAR away; guest lec

RAR away; guest lecs

RAR away; guest lecs