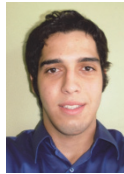
Development of a Process-Aware DFM Framework by Leveraging Test Data



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Since deep nanoscale ICs are increasing in complexity and systematic variation, there is a need to transfer more precise actionable hotspot information to the designer earlier in the design cycle to improve yield and performance. Two major contributors to systematic variation are lithography and chemical mechanical polishing (CMP). The goal of this study is to explore layout geometries which have been determined to have faulty nets by evaluating them using a simulated damascene manufacturing process. Layout snippets that contain a faulty net have actually been "virtually fabricated" by performing lithography, etching, deposition, and physics-based CMP manufacturing simulations. Consequently, full chip (snippet) fabrication is able to predict the multi-scale variations due to the processes, namely CMP, without employing the traditional pattern density methods. Since this approach would incorporate the physics of CMP, our ability to predict variation will scale with technology nodes without requiring tuning from extensive design of experiments.

In order to increase the accuracy of the hotspot detection of process variations such as those caused by CMP, this project also leverages test data. CMP hotspot predictions using this methodology are expected to have unprecedented accuracy when combined with an advanced diagnosis methodology, which has been applied to thousands of actual failing chips.

Figure 1 shows the flow for exploring a failed layout snippet using test-based diagnosis and virtual fabrication. Figure 2 shows a cumulative process hotspot map resulting from CMP-related hotspots generated at different layers during chip fabrication.

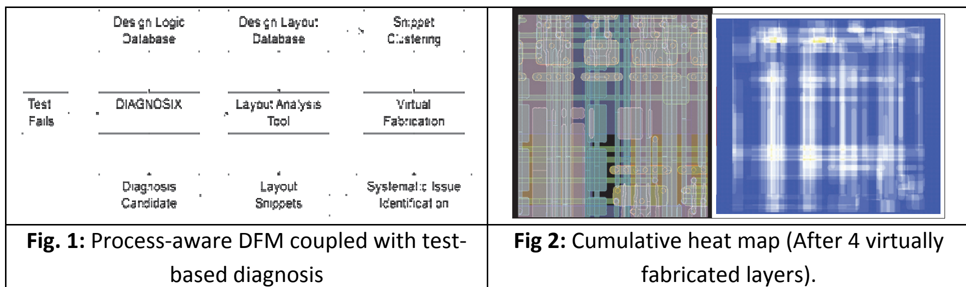

Fig. 1: Process-aware DFM coupled with test-based diagnosis	**Fig 2:** Cumulative heat map (After 4 virtually fabricated layers).