Self-Healing Current Steering DAC Design with Statistical Element Selection





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Current steering DACs (CS-DAC) are widely used for high-speed digital-to-analog conversion applications. Well matched current cells are required to achieve desired accuracy in CS-DACs. There are generally two methods to address the matching problem. The first is to rely on the intrinsic accuracy of transistors, which includes upsizing the transistors to be sufficiently large to meet matching requirements. This approach leads to extremely large circuit area for high resolution CS-DACs. The second method is to use digital or analog calibration circuits to tune the currents. Digital calibration usually suffers from very complicated system implementation, which involves a calibration loop of ADC-DSP-DAC. Analog calibration does not scale well with technology and voltage scaling. We propose a self-healing CS-DAC using Statistical Element Selection (SES) to tackle the transistor matching challenge.

The SES methodology has been successfully applied for Flash-ADC and MEMS filter designs. Unlike classical redundancy, where only one of the N available elements would be used, SES is based on selecting K elements (1 < K < N) out of N elements. This selection scheme enables an exponential number of combinations to be selected from, thereby enabling excellent calibration choices. With SES for CS-DAC design, the current cell's matching property can be greatly improved such that the total transistor area required for the desired accuracy is reduced dramatically. We have created an on-chip self-healing SES algorithm for CS-DAC design that achieves greater than 200x area reduction for current cells compared to the CS-DAC design that relies on the intrinsic accuracy of transistors. The analog circuit overhead for this SES implementation is one current comparator. The digital circuit overhead consists of a number of registers needed to store the selected combinations, and this overhead decreases with process scaling.

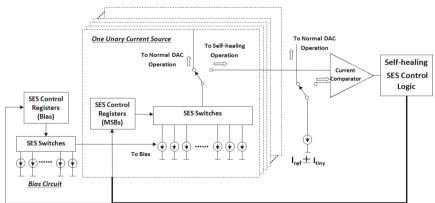


Fig. 1: Self-healing SES CS-DAC system diagram