Reliability Enhancement of Bi-Stable Physical Unclonable Functions



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Physical unclonable functions (PUFs) are die specific random functions that are used in a number of secure IC applications including unique die identification/authentication and key generation. At the core of a PUF implementation is a circuit that leverages variations in manufacturing steps to generate random bits that are unique across dies and can be reliably reproduced multiple times on each particular die across voltage and temperature variations and over aging. These bits are the source of entropy in the PUF system. The quality of a PUF implementation is determined by the evaluation of these random bits on the security metrics of uniqueness, randomness, and reliability and the VLSI metrics of area, power, and performance. While adequate randomness and uniqueness is relatively easy to achieve in most well designed PUF implementations, achieving high reliability has remained a challenge. This was confirmed from measurements on our 65nm bulk CMOS testchip. Various applications require perfect reliability and would require reliability enhancement techniques like error control coding or fuzzy extraction to increase the base reliability. However, the overhead associated with these techniques grows exponentially with error correction capability. Moreover, they may require careful implementation to avoid introduction of security vulnerabilities. Hence achieving high-reliability in baseline PUFs that result in a modest use of these techniques is critical.

In this work, we study four orthogonal and complementary techniques to enhance reliability. Our measurements show that bi-stable PUFs have far superior VLSI metrics compared to delay based designs and are therefore better candidates to trade-off some of their superior VLSI metrics to achieve higher reliability. Our analysis of reliability enhancement therefore, mainly focusses on bi-stable designs. The four techniques - multiple evaluations (ME), activation control (AC), post-manufacturing selection (PMS), and directed accelerated aging (DAA) – show an improvement of 78%, 71%, ~100%, and 40% improvement in reliability as measured by PUF response bit error rate.

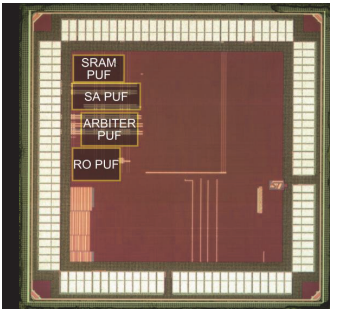

Fig. 1: Photomicrograph of 1.4mm x 1.4mm 65nm bulk CMOS testchip.

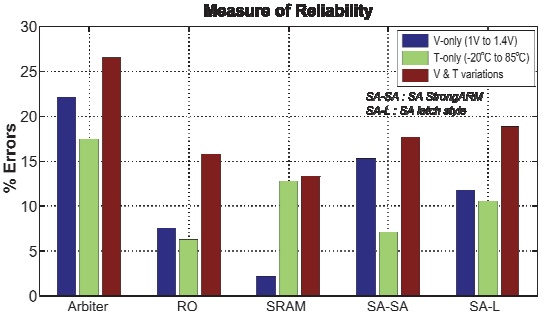

Fig 2: Reliability comparison of PUF types across voltage (V-only), temperature (T-only) and both (V&T) variations.